Self-Test Designs in Devices of Avionics

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ABSTRACT: *Avionics system with self-test designs provides the on-line detection and diagnosis to enhance system reliability for safety flight. This paper presents an example to teach students design-for-test theories and practical skills at the Department of Aeronautics and Astronautics (DAA) of National Cheng Kung University (NCKU). Self-test technologies were taught to students as an extension part of the Digital Electronics course. An Analog-to-digital converter (ADC) that is one of the significant devices in electronic circuits of avionics was used as a device under test (DUT) for self-test structure designs. This structure was divided into three circuit blocks assigned to students in groups. The blocks were specified as Test Signal Generator (TSG), Control Circuit, and Output Response Analyser (ORA). Through these projects, a novel step-ramp signal was developed as a test signal that was different from general test signals such as sinusoidal, triangular and ramp signals. According to the step-ramp signal, an effective ORA was designed to analyse the parameters of Offset Error, Gain Error, Differential Non-linearity and Integral Non-linearity. Then the test structure was configured. It was suitable for Built-In Self-Test designs with the characteristics of high precision in the step-ramp signal, simple digital circuit designs in the ORA and low chip area.*

1 INTRODUCTION

Avionics systems are popularly developed by using Very High Speed Integrated Circuits (VHSICs) and Very Large Scale Integrated (VLSI) Circuits for high complexity and high reliability designs. High complexity designs result in difficulties in circuit testing. Every avionics system eventually needs preventive and corrective maintenances. This system requires enhancing availability through rapid detection and isolation of faults. Designs for testability (DFT) techniques get the systems to be easily tested. Failures in components and modules can be effectively detected, isolated and repaired [1, 2].

Avionics system architectures are developed from component level to module level and system level. All levels are needed to include self-test designs with various technologies. Several DFT technologies are developed such as Built-In Self-Test, Boundary Scan and Quiescent Current (IDDQ) to be included in avionics systems [3, 4].

We taught DFT theories as an extension part of the Digital Electronics course [5]. Practical skills were trained through projects. Analog-to-digital converters (ADCs) were targeted as a device under test (DUT) for self-test designs. The self-test structure contained three blocks, Test Signal Generator (TSG), Control Circuit and Output Response Analyzer (ORA). Students were organized into groups of two to three members. Each student was assigned to design the circuit of one of three blocks. The details of group work included analyzing the circuit functions and performances by software, preparing and understanding the specifications of components from manufacturers' data sheet, demonstrating the functions on multi-function boards and implementing the self-test circuits and DUT on printed circuit boards.

Through the projects, the teamwork organization exhibited the effectiveness of the peer learning. Students faced the difficulties in coordination and integration of circuit interfaces in each group. The project review every other week promoted the progress of exercises and the interactions of peer learning. Groups which demonstrated good circuit designs and ideas were asked to detail their results as paradigms

for other groups. A novel test signal called step-ramp with high linearity and accuracy was developed. Based on the step-ramp signal, the test output analyzer was proposed with complete digital circuits.

In this paper, we present successive outcomes from the DFT projects. The details of the project are described in the following of this paper. The main objectives of the Self-Test circuit designs are presented in Section II. Built-In Self-Test structure is described in Section III. The concerns of Built-In Self-Test Structure are detailed in Section IV. Then the developed novel test signal and the test structure are depicted in Section V while the conclusions are given in Section VI.

2 OBJECTIVES OF SELF-TEST CIRCUIT DESIGNS

The undergraduate students at DAA without strong electronics background were targeted as maintenance and test engineers of avionics system. For self-test technologies, in addition to theoretic knowledge, the students were trained with practical skills in self-test circuit designs to achieve the following objectives:

1. Implementing the circuits with actual commercial integrated circuits;
2. Familiarizing the specifications from actual data sheets;
3. Cultivating the students' independent thinking so that they may create new ideas of self-test circuit designs.

Each group designed a self-Test structure for testing ADCs. Circuit designs in the test structure were requested to meet the requirements of low chip area, low complexity and less dependence in semiconductor manufacture processes. The test circuits within these requirements provided the benefits to implement to Built-In Self-Test structures.

3 BUILT-IN SELF-TEST STRUCTURE (BIST)

In BIST designs, test circuits used to test the DUT are embedded into a chip. The test circuits of BIST structures should contain Test Signal Generator (TSG), Control Circuit and Output Response Analyser (ORA) as shown in Figure 1. This test structure that can well develop to test chips and modules in avionics systems suits to operate on field and depot levels. In the test mode, TPG provides the test signal to the DUT. The ORA makes the pass/fail decision after it analyses the output responses received from the DUT while Control Circuits provide the control signals needed for test procedures and a regulated clock signal connected to the inputs of the TSG. BIST can be used for field level testing to diagnose the faults without the need for test equipment supports. This greatly affects the maintainability and life cycle costs of avionics systems.

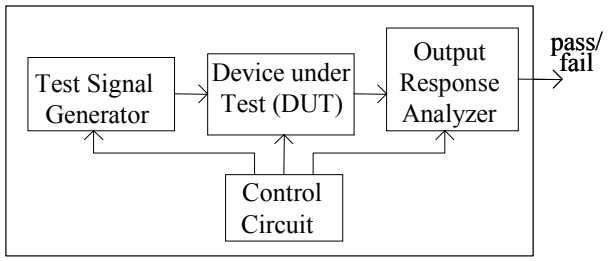

Figure 1 A basic BIST structure.

4 CONCERNS OF BUILT-IN SELF-TEST DESIGNS

Before students started to develop the test structures, they should familiarize themselves with the main issues and concerns of the following.

5 WHAT PARAMETERS WERE TESTED?

The performances of ADCs can be tested by detecting static and/or dynamic parameters. Static parameters include Offset Error, Gain Error, Integral Non-linearity (INL) and Differential Non-linearity (DNL), etc. Dynamic parameters mainly contain Settling Time, Signal- to- Noise Ratio (SNR), Total Harmonic Distortion (THD) and Effective Number of Bits (ENOB).

Analysing ADC's parameters can be executed in the time domain or the frequency domain. In the frequency domain primarily for dynamic parameter analyses, a lot of test data are first collected and stored in memory. Then they are analysed with the calculation by Fast Fourier Transform. The analyses

are done by using resources of memory and arithmetic units. The test structure for frequency domain is hardly implemented to Built-In Self-Test designs because of large chip area requirement in memory and arithmetic units.

The test structure for time domain is usually designed to analyse static parameters. Generally we can use 2^n-1 discrete multi-level voltages as test signals of n-bit ADCs. Generating accurate multilevel voltages in chips expense high costs in chip area. The operations of switching network for connecting one of multi-level voltages to the input of ADCs produce spikes when switches change from on to off states or from off to on states. The accuracy of test structure is seriously affected by spikes. To reduce the effect of switching network, the designs of novel accuracy test signals are important. The characteristics of test signals are relative to the design of the ORA that is optimally designed by digital circuits.

6 WHAT KINDS OF TEST SIGNALS WERE USED?

In addition to discrete multilevel signals, continuous signals such as sinusoidal, triangular and rising or falling linear ramp signals are prevalently used as shown in Figure 2. Sinusoidal and triangular signals make periodic waves. High frequency signals exhibit short-time variations in amplitude are always used to test dynamic parameters of ADCs. We could use a high frequency triangular wave to test dynamic parameters. However, it is more difficult to produce high frequency triangular waves with high linearity.

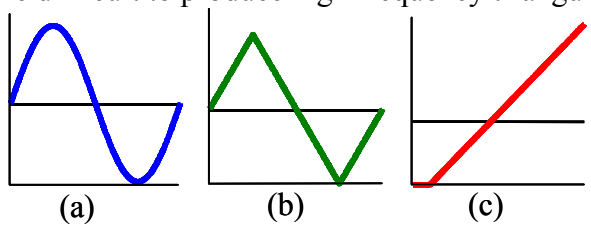

Figure 2 Continuous test signals: (a) sine wave;
(b) Triangular wave; (c) rising ramp.

The linear ramp signal as shown in Figure 2(c) is basically applied to test static parameters because the input voltage is ramped slowly. It can be easily generated by an integrator and widely used to test ADCs. Otherwise, it is difficult to generate ramp signals with high linearity for testing ADCs over 10-bit. The limitation occurs from the leakage current in capacitors that are the main components in an integrator. The higher voltage across the capacitor makes the higher leakage current. Non-linearity of the leakage current affects the linearity of ramp signals for testing high resolution ADCs.

We focused on training students circuit design skills with the platform of the self-test structure for ADCs. The test structure for static parameters generally does not need memory and arithmetic unit supports. It is much suitable for student projects with simpler circuit designs than the one for dynamic parameters. The definitions of static parameters of ADCs are described below.

Gain Error: the difference between the real and ideal voltages at the highest transition point from output code 2^n-2 to 2^n-1, where n is the resolution of ADCs.

Offset Error: the difference between the real and ideal voltages at the lowest transition point from output code 0 to 1.

Differential Non-linearity: the deviation of the analog input range that is converted to the same output code from an ideal step range.

Integral Non-linearity: the deviation of the real transition input voltage from the ideal transition voltage that is defined by the ideal transfer curve.

7 CAN THE TEST RESPONSE ANALYZER BE DIGITALIZED?

An edge code testing method is used to measure ADC parameters and to search the transfer curve between analog input test signals and digital output codes. When the changes of the output codes occur, the corresponding analog input voltages are measured to identify whether the parameters are within the acceptable ranges $\pm 1/2$ LSB (Least Significant bit). The calculation of parameters in the analog format is

less accurate and higher complex than that in digital format. The projects should meet the requirement to design the ORA in digital format. Students take a challenge on designing an analog test signal that can be accurately mapped to digital codes as references. Then the transition points of ADC's output codes can correspond to the input digital codes. The objectives of the digital ORA can be achieved.

8 THE DEVELPOED NOVEL TEST SIGNAL AND TEST STRUCTURE

The TSG works as an integrator that was composed of a differential operational transconductance amplifier and a capacitor. Three parameters (period, amplitude and duty cycle) in the regulated signal were varied via control circuits as shown in Figure 3. The difference signal between the two inputs of the integrator was integrated to become a step-ramp signal as a test signal of the device under test, ADC. The step-ramp signal can be seen as several separated ramp signals with different offset voltages. The segment integration for each separated ramp signal contributed the high linear performance. The regulated clock signal with different duty cycles overcame the problem that the high voltage across the capacitor resulted in the high current leakage.

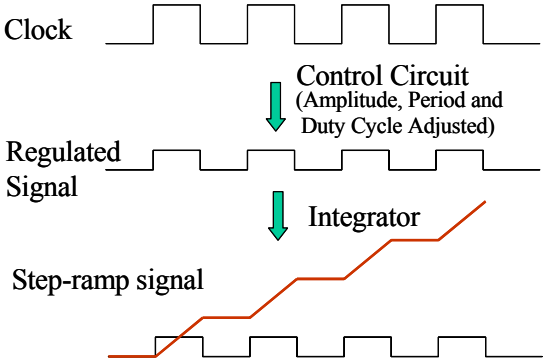

Figure 3 A step-ramp signal.

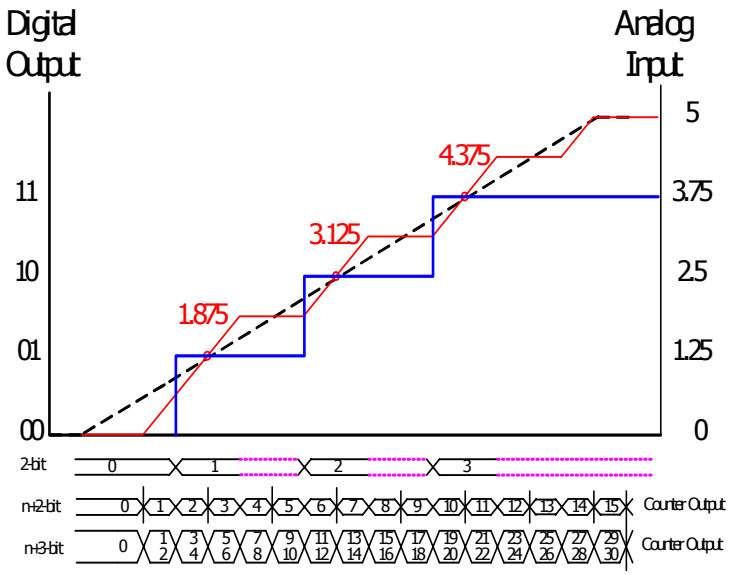

Figure 4 Step-ramp signal mapped to 5-bit counter for 2-bit ADCs.

The step-ramp signal was then synchronous with an n+m-bit counter, where n was the resolution of ADC and m=1, 2, .., based on the test precision desired. This meant that the integration time of the step-ramp signal was equal to the time of counter counting from 0 to 2^{n+m}-1. By comparing the outputs of the n-bit ADC and n+m-bit counter, the detection of parameters of ADCs was achieved. These parameters contained offset error, integral non-linearity, differential non-linearity and gain error. Figure 4 illustrated the correspondence between the step-ramp signal and the counter for the 2-bit ADCs and the 5-bit counter (n=2 and m=3).

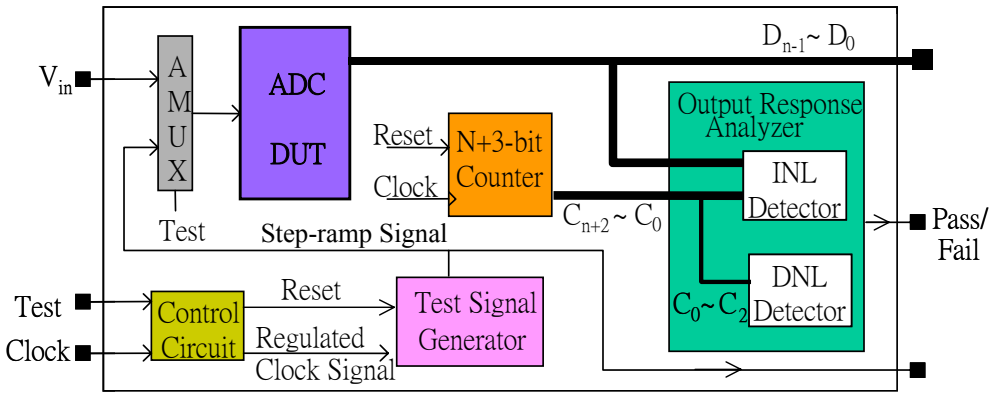

Figure 5 The configuration of BIST structure.

The configuration of the test structure was shown in Figure 5. The AMUX was an analog multiplexer used to choose either the normal input signal V_{in} when Test=0 or the step-ramp signal when Test=1. The ORA contained a DNL detector and an INL detector. The INL detector also performed Offset Error and Gain Error detections at the lowest and highest transitions of ADC's output codes. The INL detector performed the comparison between the n-bit output codes (D_{n-1}~D_0) of the ADC and the output codes (C_{n+2}~C_3) of the n+3-bit counter to identify whether the INL was within the acceptable range Only C_2~C_0 codes of the counter were needed for the identification of DNL detections. The main advantages of this test structure included:

1. The ORA was digitalized.
2. The ORA can be systematically designed based on the value of m. Simple designs in the detection circuits could be easily implemented in Built-In Self-Test structures.
3. The step-ramp signal was generated by the integrator with the input of the regulated clock signal. The n+m-bit counter was trigged by the same clock signal. Synchronization was easily achieved between the step-ramp signal and the counter.
4. Adjustable duty cycle design overcame the problem in various current leakages with different voltages across the capacitor and in deviation of integrated circuit manufacture processes.
5. Adjustable DC voltage designs in the power source of digital control circuits provided the regulated amplitude clock signal to the integrator. It was also available to overcome the problem in deviation of integrated circuit manufacture processes.

9 CONCLUSIONS

The paper presents the outcomes obtained through the exercises in projects of self-test designs for testing ADCs. A novel step-ramp signal was developed as a test signal. Based on the step-ramp signal, the self-test structure was configured. Our goals to enhance learning in theoretic knowledge and practical skills were met by the circuit design exercises. However, we also received the student's responses that they had too much work. To improve this condition, the size of groups is considered to be enlarged to include more students so as to reduce each student's work. The definition of interfaces between circuit blocks also was important for students to release the work loads and to speed up the circuit designs. Furthermore, an independent course in circuit testing was needed for learning advanced self-test technologies. The exercise experiences in the projects could be recorded and transferred to junior students. We believe that these suggestions are helpful for the improvement in teaching self-test circuit designs in the following year.

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