MORFPGA: A Modularized FPGA Development Platform for IC Design Education and Contests

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Abstract

The Chip Implementation Center (CIC), Taiwan, is a non-profit organization serving the university professors in Taiwan to realize their IC (Integrated Circuit) design projects. In order to encourage the college students in Taiwan to engage in IC design and further develop their design ability and creativity, the CIC annually co-hosts the IC design contests in Taiwan. This paper presents the design concept, development, and implementation of the MORFPGA (MORph FPGA) platform which is a modularized development platform for the design projects using FPGAs. The modularized platform provides high flexibility and expandability allowing the users to stack additional module boards. The MORFPGA platform is comprised of FPGA Core Module boards, Memory Modules, and Peripheral Module board. The MORFPGA platforms have been used for IC education curriculum development, IC design contest, and research use.

I. Introduction

The Chip Implementation Center (CIC) [1], Taiwan, is a non-profit organization serving the academia in Taiwan to realize their IC (Integrated Circuit) design projects. The CIC provides the design services, design environment, design flows, chip implementation, and measurement with no charge to the universities in Taiwan. In order to encourage the college students in Taiwan to engage in IC design and further develop their design ability and creativity, the CIC annually co-hosts the IC design contests in Taiwan. The FPGA (Field Programmable Gate Array) design contest is one of the most important measures to assess the college education in the IC design.

The FPGAs commonly used by the universities/colleges in Taiwan are either from Altera [2] or Xilinx [3]. The educational version includes only the simplified peripheral components with limited functionalities. In addition, both FPGA boards have their own salient features. In many cases, some design projects may be favorable for the users of Altera over those of Xilinx, or vice versa. As a result, the design projects and curriculum materials generally cannot be shared by different users. Further, due to the limited functionalities in common for both development boards, the design projects in annual FPGA design contests only can give much less challenging project in order to maintain the fairness to both groups of users. In addition, in the past years, the CIC offers the FPGA training courses to students during the summer and winter breaks. In general, the CIC has to develop two sets of course works and design projects to fulfill the needs of two groups of users. Resource sharing is always concerned.

In order to provide the fair design contests and to maintain high quality of design projects in the contest, the Contest Evaluation Committee has defined the required peripherals and memory modules for the future FPGA development board. Based on the design requirement, the CIC has successfully developed a modularized FPGA platform, namely, MORFPGA (MORph FPGA), for the design contest 2008. Basically, the MORFPGA is comprised of (1) FPGA Core Module board with the memory modules and (2) Peripheral Module board. Both boards have the same versatile peripherals with the enhanced functionality. The salient feature of the architecture of the MORFPGA platform is "Modularization" which enhances the expandability and reconfigurability. Users can develop their own peripheral boards and stack them on top of the basic FPGA Core Module board for other curriculum development or for research use.

In the next section, the design requirement for developing the MORFPGA platform is discussed. We will first describe the format of the FPGA design contests, and then present the design project in 2007 design contest to outline the difficulties for providing a fair contest with a higher quality project. Finally, the design specification defined by the Contest Evaluation Committee is discussed. Section 3 presents the system implementation and detail design. Section 4 assesses the effectiveness of the MORFPGA platform for 2008 design contest. The contest results in the past years are compared and evaluated. Finally, a concluding remark is given in Section 5.

II. Design Requirement

2.1 Design Contest

The FPGA design contest encourages undergraduate junior and/or senior students to organize a design team to participate. The design contest is a two-step process: Preliminary Contest and Final Contest. The Contest Evaluation Committee generally selects the best 30 design teams who have completed the design project within the duration of 12-hours in the Preliminary Contest. Then, the selected teams are gathered at the CIC classroom for the final contest, as shown in Fig. 1. The finals will be awarded with a certificate and an attractive prize given from the Ministry of Education, Taiwan. The certificate is highly recognized by the IC industrial in Taiwan. With the certificate, students can easily get the job interview opportunity when they are graduated.

Fig. 1 FPGA Final Contest in 2008.

The preliminary contest is completely open to all undergraduate seniors and juniors who are encouraged to organize a design team, two members in each team, to participate the design contest under supervising by a professor from their university. Each team is enrolled to receive the account with password to download the design project. Every team can take the design project, posted by the CIC, including the design problem, design specification, and the functional test vectors.

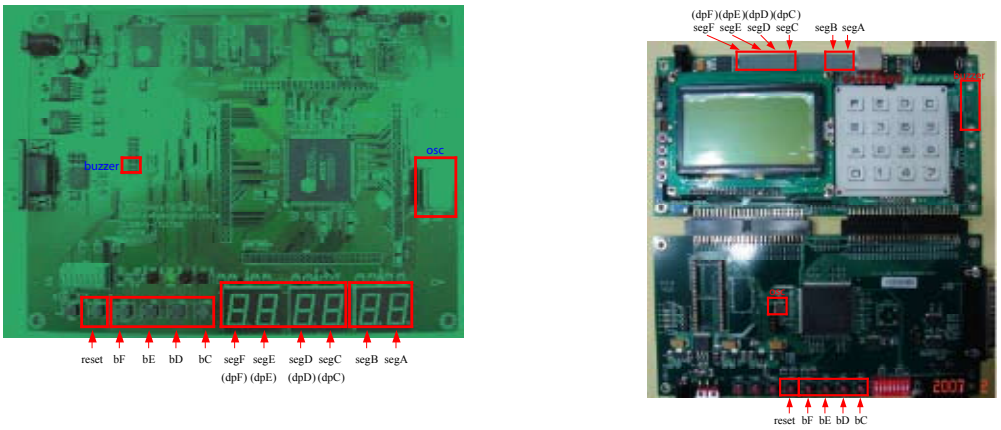
Note that the Preliminary Contest attempts to test whether the design teams really understand the basic integrated circuit design and FPGA design flow provided by the CIC. Thus, on the date of the Preliminary Contest, each design team has a duration of 12-hour to download the design project, study the design specification, work on the design project, and upload the design file including RTL code, testbench, simulation results, etc. All design teams are working on the design projects in their own laboratories with the same design environment, as listed in Table 1, provided by the CIC. In this stage, each design team is only required to complete the logic design and verification using functional simulation. It is not necessary to port the design to the FPGA development board. According to the selection criteria on design quality and upload time, the Contest Evaluation Committee selects the best 30 design team for the Final Contest. Since all design teams have the same design environment provided by the CIC, the Preliminary Contest is very fair to all design teams.

Table 1. Design Environment for Preliminary Contest

HW Description Language	Verilog_BVHDL
Circuit Simulator	Mentor Graphics ׀ ModelSim (v5.8 SE)
Circuit Synthesizer	Mentor Graphics ׀ Precision Synthesizer (v2005c)
FPGA Implementation	Altera ׀ QuartusII (v6.0)_BXilinx ׀ ISE (v8.2i)

For the Final Contest, the selected design teams also have duration of 12 hours to complete the design project with the design environment, as listed in Table 1, and the development boards, as shown in Fig. 2. All design teams are required to port their design to FPGA development board for demonstration.

Fig. 2 FPGA Development Boards for Design Contest 2007.



(a) Altera ACEX 1k EV Board

(b) Xilinx Spartan3 EV Board

Once the design project is completed, the team will demonstrate their design to the Contest Evaluation Committee. If the correctness of the design project is verified, the team will hand in the design data including the design document, original design file, and simulations results. The committee will record the performance and the completion time. Once the design data is turned in, they are not allowed to modify any more. However, if the team fails to the demonstration, each team has one more chance to re-design the project.

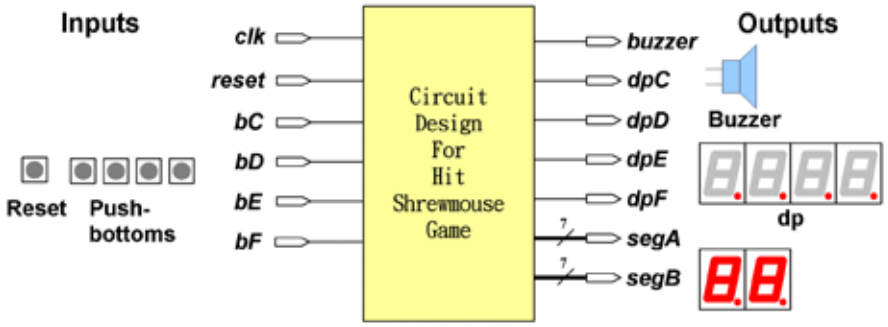
2.2 Design Projects for Design Contests

Both FPGA development boards in Fig. 2 are commonly used in Taiwan for the FPGA design education. The education versions include only the simple peripherals with the limited functionalities. Because both FPGA boards have their own salient features, some design problems may be favorable to Altera over Xilinx, or vice versa. Due to the limited functionalities in common, the design projects in the previous FPGA design contests were much less challenging in order to maintain the fairness to both groups of users.

More specifically, the “rhythmic light flash” design project was on the top list of candidate project for the 2007 FPGA design contest. The project requires the peripherals at least include one clock input, four push-bottoms (for control the flat node, sharp node, read data, and reset), and at least eight 7-segment display. However, the available peripherals of the FPGA development board in Fig. 2(a) include six 7-segment displays, five push-bottoms, while the FPGA board in Fig. 2(b) has eight 7-sgement displays, 4 push-bottoms, one keypad, and one 16x2 text LCD monitor. Apparently, both development boards have insufficient peripherals to realize the design project.

Furthermore, the same RTL code with the same logic synthesis process may result in different functions when the different boards are used. With different peripherals and functionalities, it would be very difficult to come up with a design project which is fair to both board users. Finally, a less challenging “hit shrewmouse” design project was given for the design contest. The project requires one clock input, 5 push-bottoms, and six 7-seqment displays, as shown in Fig. 3, and can be realized by both boards.

Fig. 3 Block Diagram of Hit Shrewmouse Design Project



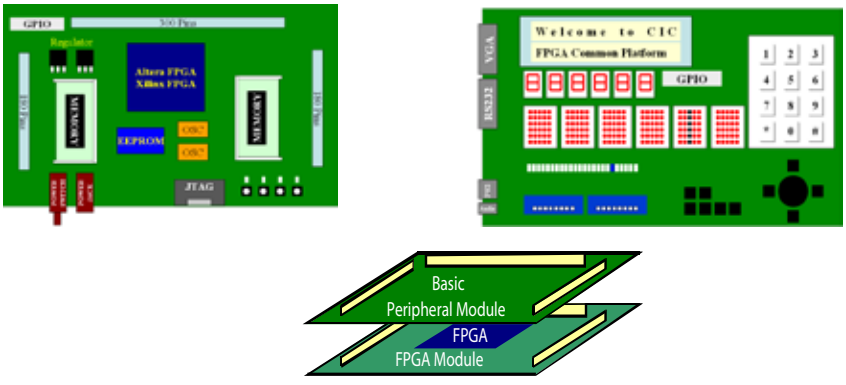
When the decimal point (dp) light of each 7-segment display is turn ON or OFF, it is indicated the appearance or disappearance of the shrewmouse. Four 7-segement displays are used in this game. The four push-bottoms correspond to the four dp points. If a dp is ON and the corresponding push-bottom is pressed, it is indicated the shrewmouse is hit, the buzzer sounds, and the counter realized by two 7-segements adds one point. No point is given if the push-bottom is pressed after the dp is OFF. Apparently, the design project is much less challenging and also favorable to the Altera's users, because the Xilinx's users need the extra efforts to handle the scan-based 7-segement displays.

III. Development – MORFPGA Platform

3.1 Basic Development Concept

The MORFPGA is comprised of two types of module boards: FPGA Core Module board and Peripheral Module board [4]. Fig. 4(a) shows the block diagram of the FPGA Core Module board. It includes the FPGA and its corresponding serial configuration device, LEDs, Buttons, GPIO, JTAG, and memory modules. Fig. 4(b) illustrates the Peripheral Module which includes LCDM, Switches, Buttons, Keypad, 7-segment displays, Dot Matrix, RS232, VGA, PS/2, and Audio. Finally, the peripheral module board is stacked on top of the FPGA Core Module board as shown in Fig. 4(c).

Fig. 4 Design Concept:
(a) FPGA Core Module Board; (b) Peripheral Module Board; and (c) Integrated FPGA Platform.



(a) (b) (c)

3.2 Design and Implementation of MORFPGA Platform

Fig. 5(a) shows the Xilinx FPGA Core Module board which is implemented with the Xilinx FPGA chip and the associated serial configuration device (XCF16P). The FPGA chip has 1.5M system gates, or approximately 30 K logic cells, 208K distributed RAM, 576 block RAM (each block contains 4K bits), and 487 user I/O pins. Simi-

larly, Fig. 5(b) illustrates the circuit implementation of the Altera FGPA Core Module board realized with Altera EP2C35F672 FPGA chips and the serial configuration device (EPCS16).

Fig. 5 Module Board: (a) Xilinx FPGA Core; (b) Altera FPGA Core; and (c) Peripheral.

(a) (b) (c)

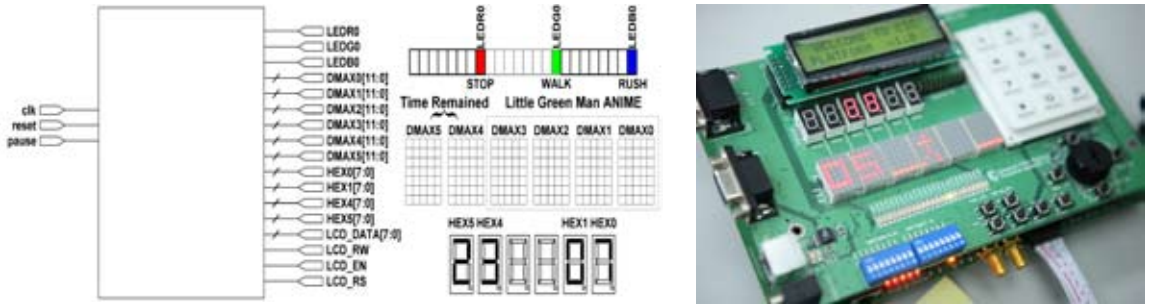
The memory modules include 4Mb SRAM (256Kx16), 512 Mb SDRAM (8Mx16x4 Banks), and many others [5-9]. In order to enhance the flexibility of using whatever the memory modules needed by the users, a SODIMM (Small-Outline Dual In-Lin Memory Module) [10] was adopted and integrated. The appropriate memory module can be plugged to the SODIMM module. In this implementation, the SODIMM module is placed on the back side of the FPGA Core Module board. The Peripheral Module board, as shown in Fig. 4(b), is designed and implemented, as illustrated in Fig. 5(c). The module includes a 16x2 LCDM, DIP Switches, Button Switches, Rotary Push-bottom Switch, Keypad, User Pins, six 7-segment displays, six 5x7 Dot matrix displays, RS232, VGA, PS/2, and Audio. Finally, the SAMTEC [11] high-density connectors are used for interface between boards.

IV. Assessment

4.1 Design Project for 2008 FPGA Design Contest

In 2008, the FPGA design contest adopts the MORFPGA as the development board for the Final Contest. The design project was entitled, "Pedestrian Traffic Signal Controller °V Little Green Man." The design project is to imitate the pedestrian traffic signal. Fig. 6(a) shows the block diagram of the design project. The circuit takes three 1-bit input signals, reset, clk, and pause. As their names imply, reset and clk are the reset and clock signals, while pause is to temporally suspend or toggle the mode.

Fig. 6 Block Diagram of Design Project and MORFPGA Platform.



(a) (b)

The 2008 Contest Evaluation Committee set up the following criteria to evaluate the design quality: (1) When the system is powered ON, the anime patterns for STOP mode is played, check if all display devices show the correct answer; when the pause is enabled, whether the timing information displayed in the 7-segment display as defined is exactly the same as that debug information displayed at the LCDM; whether the LEDR0 is lighted up, and when the reset is enabled, check if the system is actually reset; (2) Repeat Item (1) for WALK mode; (3) Repeat Item (1) for RUSH mode; (4) Check if the system enters the STOP mode right after the RUSH mode; (5) Check if the cycle

STOP-WALK-RUSH is repeated in a correct order; and (6) Check if the de-bounce is properly designed for the push buttons. Fig. 6(b) shows the partial demonstration of the design project.

4.2 Assessment

Apparently, the design project described above for "Green Man" is much more challenging than the Hit Shrewmouse Design Project in Fig. 3. This is so simply because the MORFPGA platform has much more peripherals for more challenging design projects. This section is to assess the effectiveness of using the MORFPGA platform for the FPGA design contest. The assessment will base on the executing results of the last three years. The FPGA development boards in Fig. 2 were used for the design contests of 2006 and 2007, while the MORFPGA were used for that of 2008. The design projects for these three years are respectively

2006: "ßPseudo-random Integer Sorting Circuit"
2007: "ßHit Shrewmouse"
2008: "ßPedestrian Traffic Signal Controller°VLittle Green Man"

One may evaluate whether the design project is challenging by counting the number of teams which completed their project within the time duration. Table 2 lists the completion times of the design projects in the Final Contests of the last 3 years.

Table 2. FPGA Design Contest – Completion Time
(Final Contest)

Completion	**2006**	**2007**	**2008**
After 1 hour	0	1	0
3 hours	5	5	0
5 hours	12	5	0
7 hours	9	2	0
9 hours	5	4	3
11 hours	2	5	2
12 hours	0	0	1
Incomplete	9	8	23
Total Teams	42	30	29

Table 2 shows that there are only 6 teams who have completed the design project within the duration of 12-hours, while there were 24 and 22 teams in 2006 and 2007, respectively. In particular, 5 and 6 teams even completed their design projects within 3 hours. In 2008, the fast design team took 9 hours to complete their design project, while 31 and 17 teams completed within 9 hours in 2006 and 2007, respectively. The results show that the design project in 2008 is much more complicated than those in previous year. This is so simply because the MORFPGA allows developing more challenging design projects.

V. Conclusion

This paper presents the design concept and development for the MORFPGA platform which is a modularized development platform for the design projects using FPGAs. The modularized platform provides high flexibility and expandability allowing the users to stack additional module boards. For example, at time of this writing, the available FPGA Core Module boards are from Altera and Xilinx, one can replace them by other vendors' FPGA chips; the memory module boards can be easily updated with the advanced memory chips; the Input devices in the Peripheral Module board can be modified using more advanced devices such as touch panels; one may add the Peripheral Module board including ARM-based SoC platform to enhance the functionality for research use, and etc. The above mentioned features are being developed by the CIC.

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