Education on CMOS IC Design and Reliability

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Abstract — *With the exploding development of wireless communications, RF education needs to be improved accordingly. This paper describes a proposal to build or improve the courses for senior and graduate students to learn the CMOS integrated circuit design and reliability for wireless communications. Traditional textbooks do not cover CMOS reliability for the design of RF circuits using today's nanoelectronic technology. For effective learning, students first need to know how hot electrons and gate gate oxide breakdown occur. The experimental data of stressed devices are then demonstrated for further understanding. Using stressed transistors data and RF device model, RF circuit performances subject to stress are examined. Hot carrier effect and gate oxide breakdown increase noise figure and decrease power gain of MOS transistor circuits. From physical insight into RF circuit degradation, one can design RF circuits to reduce hot electron and oxide breakdown effects on circuit performance. This flow provides a robust circuit design and is essential in today's wireless integrated circuit design and education. A systematic study of RF circuit performance degradations due to hot carrier and soft breakdown effects is reported. The experimental facts of DC stress on the RF properties of MOSFETs are given. The methodology to study the HC and SBD effects on RF circuits is proposed. The performance degradations of a low noise amplifier are examined using the methodology developed.*

Index Terms — *CMOS, integrated circuits, reliability.*

1. INTRODUCTION

Today's electronic products in wireless communications require low power dissipation and longer lifetime of battery. Silicon CMOS is the key semiconductor technology to produce high-density integrated circuits with low power dissipation for portable electronics. High speed and high frequency operation of electronic systems and circuits are essential for data/voice transmission for the information age.

When CMOS device sizes are minimized to achieve high density, the channel electric field of MOS transistors becomes higher. This enhances hot carrier (HC) effects. Furthermore, the scaling of oxide thickness could trigger the gate oxide soft breakdown (SBD). As a result, reliability issues in CMOS devices and circuits become very important [1] [2]. Degradation of the DC device parameters has received widespread attention, and the degradation of RF circuit performance has not been studied systematically.

Traditional textbooks do not cover CMOS reliability for the design of RF circuits using today's nanoelectronic technology. For effective learning, students first need to know how hot electrons and gate oxide breakdown occur. The MOSFETs are stressed to show the HC and SBD effects. Using stressed transistors data and RF device model, RF circuit performances subject to stress can be simulated. It will be seen that HC and SBD increase the noise figure and decrease the power gain of MOS transistor. From the physical insight into RF circuit degradation, one can design RF circuits to reduce hot electron and oxide breakdown effects on circuit performances. This provides a robust circuit design flow and is essential in today's wireless integrated circuit education.

In this paper, a systematical design of a course on CMOS IC and reliability is described. In section 2, the course design is described. In section 3, HC and SBD effects on MOSFETs and RF ICs are examined. A typical transceiver block, low noise amplifier (LNA) is taken to show the CMOS IC design and reliability issues. LNA performance degradations due to HC and SBD effects are shown. The conclusion is given in Section 4.

2. COURSE DESIGN

The CMOS IC design and reliability course is an interdisciplinary course, including microwave, microelectronics, and semiconductor physics. It is composed of two parts: the lecture and the laboratory. The lecture is mainly to provide the students the basic concepts and design techniques in RF IC design and reliability, and in the laboratory, the students need to do stress experiment and design their RF circuits using some IC design tools, including simulation and layout. Because it is designed to be finished in one semester, the course is concentrated on letting the students to grasp the basic RF IC design techniques and study HC and SBD effects on CMOS RF IC using CAD tools. The prerequisite for beginning the CMOS IC design and reliability course is completion of the undergraduate electromagnetics course, semiconductor theory and the undergraduate electronic circuits.

2.1 Lectures

In addition to provide the basic RF theory and design techniques, the lecture needs to cooperate with the laboratory to make the students grasp the essential RF design theory and skills. The lecture is composed of mainly two parts: IC technologies and RF circuit design techniques.

CMOS device theory is essential for the students to understand some RF IC design techniques and reliability issues. With the continuous increase of the working frequencies and decrease of the device sizes, the RF IC design techniques are experiencing great changes. The scaling effect and device noise properties are so important that they affect the RF circuit performance greatly. Therefore, the MOSFET device theory is critical and should be covered in the course.

Therefore, beside the IC technologies, the lecture on CMOS RF IC design techniques and reliability should include following:

1) Review of transceiver architectures, functionality and main parameters for each block. This part can give students a whole picture of the transceiver, main parameters for the receiver and transmitter, and the relationship between the block parameters and the transceiver parameters.
2) Mechanisms of HC and SBD effects. There are several physical mechanisms about HC and SBD effects. Students need to understand how HC and SBD effects occur with the continuous decrease of MOSFET sizes. One common model for HC effect is the 'lucky model'. Those models can be confirmed by the students in the experiments.
3) Basic concepts of RF IC design:
   For most blocks in the transceiver, the most important parameters include:
   a. Noise performance. Noise figure (NF) is a measurement of the noise performance for each block. For VCO and frequency synthesizers, phase noise needs to be as low as possible.
   b. Linearity. To measure the linearity of each block, 1-dB compression point and IP3 can be used. Two-tone test is used for IP3 measurement.
   c. Impedance matching. S-parameter and Smith chart can be used for the input and output impedance matching.
   d. Gain and dynamic range.
4) Circuit design techniques:
   The block circuit design techniques are lectured one by one, including main parameters for each block, what circuit configurations can be used to achieve the required parameters. For example, in a low noise amplifier (LNA) design, low noise, high linearity, and good impedance matching are more important than other parameters. To achieve those performances, different circuit configurations can be used. One specific configuration, common source amplifier with a degenerated source inductance, for example, can be used to demonstrate how to analyze and design the circuit and how to control/tune-up the main parameters.

2.2 Experiments

Experiments play an important role in this course. To examine the HC and SBD effects, students need to do stress experiment. Because HC and SBD are both accumulation process, the MOSFETs have to be overstressed to show HC and SBD effects. In our experiments, the devices used are 0.16 μm CMOS transistors. The gate oxide thickness is 2.4 nm. The wafers are tested with the Cascade 12000 Probe Station and Agilent 4156B Semiconductor Parametric Analyzer for DC measurements, while the RF experiments up to 50 GHz are carried out using Agilent 8510C Network Analyzer. Oxide stress and channel hot carrier effects are applied to the transistor simultaneously to mimic the circuit operation condition while the source and body is grounded. To get worst case HC and SBD effects, the accelerated stress condition is carefully set at $V_G = V_D = 2.6$ V.

Equipments in the experiment include: HP 8510C network analyzer, HP 8517B(45MHz-50GHz) S-parameter test set, HP83651B(10MHz-50GHz) 8360B series synthesized sweeper, Summit 12751 Cascade Microtech probe station, and related software.

Typical setup for network analyzer measurements at the probe tips connects the HP 8517B test set through cables to the probe heads, as shown in Figure 1.

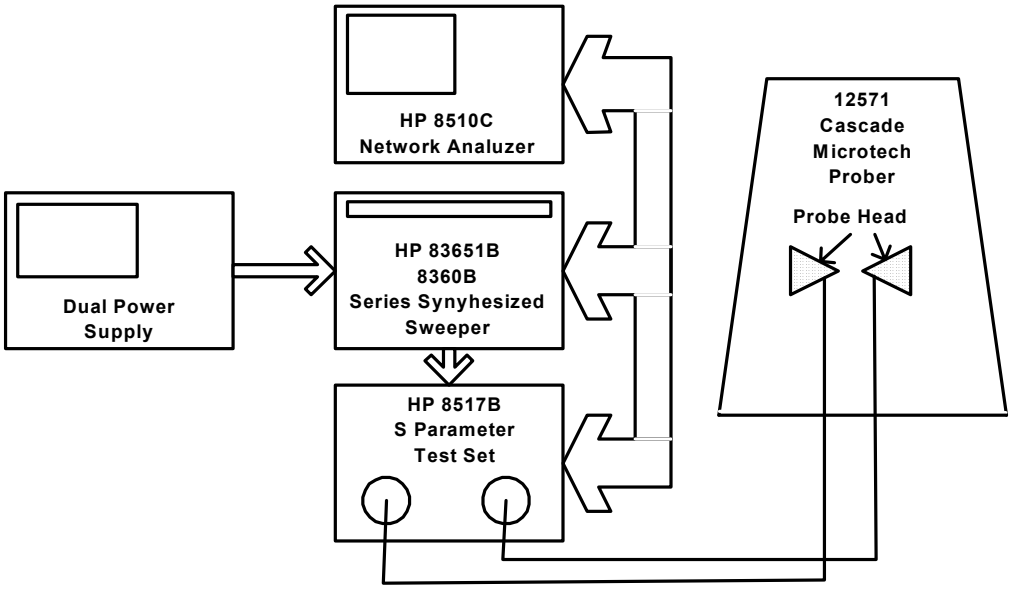

Figure 1 On-wafer measurement system

Some aged device models are extracted from the experiment, and used to simulate RF circuit performance degradations due to HC and SBD effects. Some examples are shown in next section. The students can use Cadence SpectraRF or ADS to simulate performance degradations of RF circuits.

3. HC and SBD Effects on RF IC

With the continuous decrease of the MOSFET sizes, the electric field in the channel become much higher, which causes hot carrier effect. Some carriers in the channel can gain very high energy. Some of them could go through the gate oxide and get trapped in the oxide, which could make device parameters drift, and in turn, degrade the RF circuit performance. The devices used in our experiment are 0.16 μm MOSFETs with the gate width of 50 μm, the gate oxide thickness of 2.4 nm, and the threshold voltage of 0.4 volt. The measured device parameter degradation can be seen in Fig. 2. To enhance the hot electron degradation, the accelerated stress condition is set at $V_g = V_d = 2.6$ V. From Fig. 2, the threshold voltage and mobility degradations are about 40% and 45%, respectively; the transconductance and cut-off frequency degradations are about 27% and 43%, respectively. The students use the MOSFET parameter degradations to evaluate the RF circuit performance degradations due to HC effect. They can apply the extracted aged model files to the RF circuit they designed, and see the HC effect on the RF circuit performance.

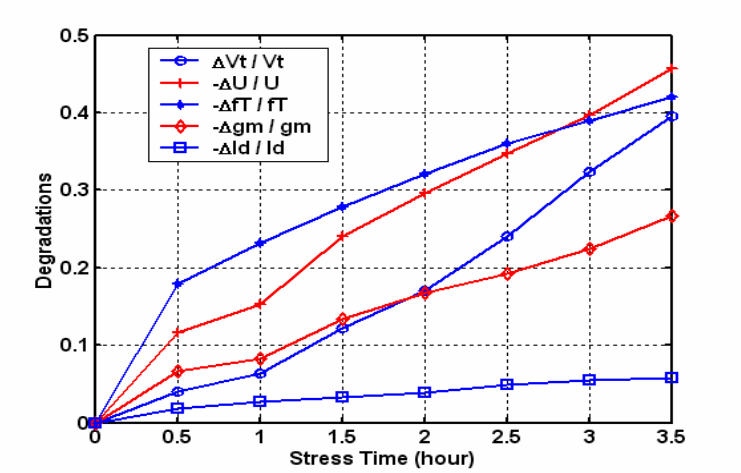

Figure 2 Measured MOSFET parameter degradations

To show HC and SBD effects on RF IC, consider one of the course projects, the design of a CMOS low noise amplifier for WirelessLAN application. The IC design tool is CADENCE and SpectraRF simulator.

To evaluate HC and SBD effects on this LNA performance, the 0.16 μm NMOS device is stressed and the degraded device parameters are extracted and applied to the LNA circuit. The basic LNA circuit is shown in Figure 3, and the LNA S-parameter degradations due to HC and SBD effects for BlueTooth application are shown in Figs. 4 to 6. It is shown in Figure 4 that the LNA deviates from the matching point after stress. This is because of significant changes in the equivalent input components of the transistor such as C_{gs} and g_m that tend to degrade the input impedance matching dramatically. In Figure 5 both magnitude and the phase of S21 are degraded, which is mainly due to the g_m decrease of the transistor. And in Figure 6, the output matching is also degraded.

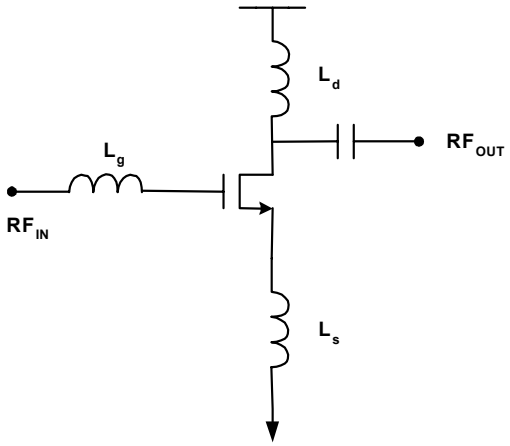

Figure 3 Schematic of the basic LNA

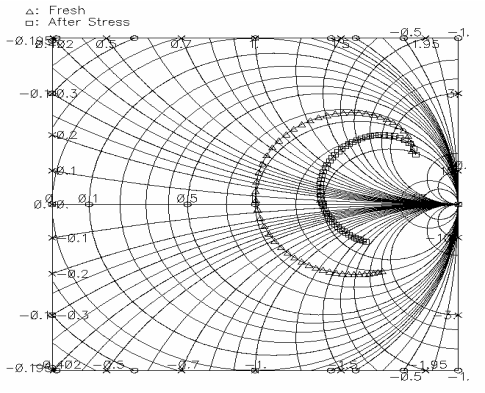

Figure 4 S11 degradation

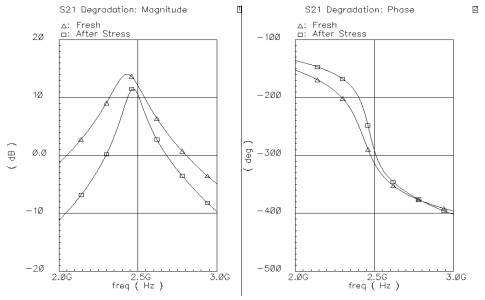

Figure 5 S21 degradation

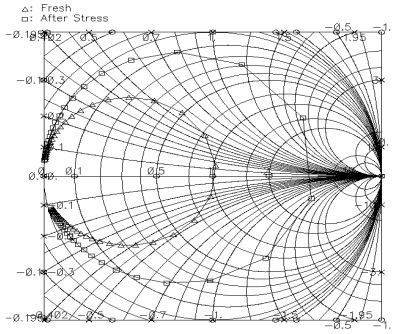

Figure 6 S22 degradation

4. Conclusion

Education on CMOS IC design and reliability is systematically discussed. A new graduate level course on CMOS RF IC design and reliability is proposed. Both lectures and experiments are discussed. This course will help students understand the mechanisms of reliability issues and learn techniques to improve the IC design in reliability.

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