VLSI Education Improvement Programs for Technological and Vocational Colleges in Taiwan — Opportunities and Challenges

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Abstract — Envisioning system-on-chip design as the next industrial evolution, the Taiwan government recently launched a national Si-Soft project aiming to improve the infrastructure for the SOC based high-tech industry in Taiwan. The fabric of the Si-Soft project is the manpower development. The potential human resources in the TVE systems are thus considered as the best supply to achieve the goal of strategic man power growth. With this regard, six university alliances for promoting the VLSI education programs in Taiwan have been founded under the supervision of MOE. One of the alliances named "prototyping & layout alliance (or P&L alliance)", is primarily designated for the technological and vocational education (TVE) schools. In the first phase of program implementation, the P&L alliance has proposed 4 tracks of courses to help the TVE schools build up their VLSI curriculum. They are 1) FPGA based design and system prototyping 2) IC back end design & layout engineering 3) high speed PCB design and 4) automatic test equipment practices. With the joint efforts of both academia and industry, the lecture materials of these courses were compiled and then promoted in the alliance schools. The MOE of Taiwan government also subsidizes the alliance schools to set up the teaching laboratories. The program goal is to educate students with practical knowledge and techniques closely related to the industry practices. In addition, the alliance also provides training programs for those faculties wishing to transfer to the arena of VLSI education. In the second phase of the program, advanced topics such as system on programmable chip (SOPC) and application specific layout will also be implemented. In this paper, we will first overview the current status of VLSI education in TVE schools in Taiwan. We will next present the alliance program and address the problems encountered as well as the measures adopted. Finally, some preliminary results and future look of the program are presented.

Index Terms — technological and vocational education, VLSI curriculum, high tech man power, education renovation program.

INTRODUCTION

During the past few years, technical institutes and science & technology oriented universities in Taiwan have been rapidly developed. The total student enrollment has exceeded two hundred and seventy thousand by the year of 2001. This accounts for about 39% of the total college students, including both regular and technological systems [1]. Despite of its large man power, the technological and vocational education (TVE) system in Taiwan did not play a due role in the high-tech industry. For years, the TVE system in Taiwan has been considered as inferior to the regular university system in Taiwan. To a very high percentage, the students entering the TVE system schools are those who failed in entering the schools in regular system. On the other hand, except for the national universities of science & technology and few newly established private schools, most colleges in the TVE system, in the past, were both under-staffed and under-facilitated. As a result, many graduates from the TVE schools are considered as unqualified for the jobs in their specialties. From the educational point of view, this is regarded as a big waste in highly educated man power. How to renovate the TVE system so that most graduates are well trained for their professional career is thus an urgent topic.

The high tech industries in Taiwan, mainly based on personal computers, consumer electronics and IC foundry, have been prosperous in the past two decades. They, however, are facing more and more challenges from other developing countries and are suffering from the decrease in profit margins. Envisioning system-on-chip (SOC) design as the next industrial evolution, the Taiwan government recently launched a national Si-Soft project (National SOC project of science & technology) aiming to improve the infrastructure for the SOC based high-tech industry in Taiwan. The background of the Si-Soft project [2] is that Taiwan has performed very well in IC foundry, design and testing. It is about the time to have another industry leap by developing a so called knowledge based industry. SOC, as a driving force to integrate hardware, software and system designs into a single silicon platform, is thus considered as an appropriate vehicle to carry out the third wave of high tech industry revolution in Taiwan. The Si-soft project includes many working items. One of the working items is the manpower development to support the strategic growth in the SOC industry. The manpower development is undergone into
two arenas, i.e., industry and academia. Due to the large manpower demand, the potential human resources in the TVE systems are thus considered as the best source to be exploited.

VLSI Education in Taiwan’s TVE System Schools

The essence of the manpower development in schools is to create specialized curriculum, develop appropriate teaching materials and train more qualified faculties. In this regard, six university alliances for promoting the VLSI (very large scale integrated circuit, the fundamental of SOC) education programs in Taiwan have been founded under the supervision of consulting office, MOE (minister of education). In particular, one of the alliances named “prototyping & layout alliance” (or P&L alliance in short), is primarily designated for the TVE schools. Actually, likewise VLSI education renovation programs have been carried out for more than 8 years. In the past, most of the participated schools came from the camp of regular universities. The program turned out to be very successful. The TVE system schools in Taiwan did not actively participate in this program until 3 or 4 years ago. Aiming to pass the MOE’s evaluation and upgrade to university or institute of technology, many TVE junior colleges hired a lot of PhD graduates in the past few years to strengthen the research of their faculties. Many of these faculties were from the regular system schools and specialized in VLSI design. Naturally, they helped set up the VLSI programs in their schools and started to involve in the program.

The statistics figures coming from the chip implementation center (CIC), national science council of Taiwan can show the trend of active participation from the TVE schools. CIC is an NSC sponsored national laboratory similar to the MOSIS organization in the US. Its missions are primarily to serve the academia in three areas, i.e. 1) IC and system design services 2) chip implementation and testing services, and 3) training program and technology exchange/proliferation. It also helps academia purchase industry compatible EDA (electronic design automation) software at subsidized prices to set up their IC design environment. Therefore, some of the CIC’s statistics may reveal, in partial, the current status of VLSI education in Taiwan’s TVE schools. Figure 1 shows the number of schools in both regular and TVE systems ever purchased EDA tools through the CIC. This implies that these schools are offering some form of VLSI courses to their students and therefore need the EDA tools to support their teaching. The schools in each system are further divided into three categories, i.e. national, private and junior colleges (for TVE system only). A total of 54 TVE schools (including junior colleges, institutes of technology, and universities of science & technology) are involved. According to the MOE’s data, there are 86 TVE schools (junior colleges or above) in Taiwan by the year of 2002. The percentage is roughly 63%. This number can be even higher if we exclude those TVE schools with focused specialties, e.g. nursery or business schools. Figure 2 gives the comparison in the student attendance of CIC offered training courses. These courses are dedicated for specific EDA tool training and the students attending these courses can be considered as engaged in some stages of IC design. Even though the attendance of TVE system students has been steadily increased these years, the pace, however, is somewhat slower than that of the regular system students. Note that TVE system students account for 39% of the total college student population. There is definitely a large room for further VLSI education program promotion in the TVE system schools. Figure 3 shows the annual data of IC chips designed by the TVE system schools and implemented through the CIC services. According to the guidelines of CIC, chips for educational purpose with constrained die size and packaging are automatically qualified for the implementation service free of charge. Chips for research purpose demanding large die size and complex packaging are subject to project evaluation before the chips can be implemented. It is quite obvious that most of the designs submitted by the TVE system schools are for educational purpose and the growth has been significant in the past few years. The number of research oriented chips still falls far behind. This is probably due to the under-developed graduate programs in the TVE system schools. For years ‘01 and ‘02, the growth, however, was considerable. Figure 4 shows the comparison between the two systems. Despite the growth in the TVE system, the schools in the regular system apparently advance more swiftly.

To understand the current VLSI education status in the TVE system schools, the P&L alliance also conducted a survey within its allied schools. The questions of the survey are classified into three categories, i.e. 1) the percentage of the VLSI related faculties in the department 2) the percentage of the VLSI-major students in the department and their status after graduation 3) the VLSI related courses offered in the department. A total of 11 schools responded to the survey. The profiles of these schools are listed in Table 1. About half of them are universities and half of them are colleges (institutes of technology). It is generally recognized in Taiwan that universities of science & technology have more research activities and resources than the institutes of technology have. As for the specialties of the responding departments, nine of them are electronic engineering, one is computer & communication engineering, and one is computer science. The number of each year’s new undergraduate enrollment ranges from 55 to 360. Six of these departments offer graduate programs (MS or PhD) and each year’s new enrollment ranges from 8 to 77. It should be noted that most allied schools are either with well established VLSI program or plan to do so. Therefore, the survey results may not faithfully represent the whole picture of current VLSI education in Taiwan’s TVE system schools. Most likely, the results indicate an over-optimistic estimate. Table 2 summarizes the survey results of category 1 and 2. All the numbers in the table are the weighted average of each school’s data. From the table, about 14% of the faculties in EE (electronic engineering)/CS (computer science) departments of the
TVE system schools specialize in IC design / EDA or testing -- the specialties exactly match the needs of the Si-soft project. About the same percentage of faculties specialize in semiconductor devices or IC fabrication process. We purposely include this portion of manpower in our survey because their specialties are closely related to the IC design and the efforts of switching their specialties to IC design are moderate. Therefore, they can be regarded as the potential manpower yet to be exploited. About one third of the senior students in these schools choose VLSI as their major. This means that they either work with a VLSI majored professor on their senior projects or take courses mainly from the VLSI program. The percentage is considered as relatively high with regard to the wide varieties of the fields in electronic engineering. This is partially due to the prevailing image in Taiwan’s society that people working in IC design companies are very well paid and compensated with large bonus. In B.2 entry, the number shows that about one third of the EE students in TVE system school continue to work on the master degrees. There is no statistics to tell how many of them are VLSI majored. If we assume the ratios of students entering graduate schools are equal in all EE majors, then about one third of the VLSI majored undergraduates choose to pursue a higher degree. Another one third (13.1% vs. 32.5% from B.3 entry) students find an IC related job. The remaining one third students either work on unrelated jobs or are still serving their compulsory military services (the term is 2-year long in Taiwan). It is estimated that the percentage of this portion of students is much higher in those less prestigious TVE schools. With adequate VLSI curriculum, these students can be turned into potential manpower for IC designs. As for the graduate (master) students, from Table 2 entry C.1, about 30% of them are VLSI majored. This is about the same percentage as that in the undergraduate case. From the number in entry C.2, about 22% of the master graduate work on VLSI related jobs. The ratio (22.1% vs. 30.9%) is significantly higher and approaches 70%.

The survey results of VLSI related courses offered in the EE/CS departments of the allied schools are shown in Figure 5 (for undergraduate) and 6 (for graduate), respectively. In the undergraduate program, three basic courses, i.e. introduction to VLSI design, FPGA (field programmable gate array) design, and HDL (hardware description languages) are offered almost in every department. Less than half of the schools support more specialized topics such as analog IC design, computer aided design (CAD) and IC testing. As for the graduate level courses, the fundamental digital and analog IC design courses are offered in all schools (6 out of 11 allied schools have graduate programs). Advanced topics such as testing and design for testability (DFT), SOC design, RF IC, and Silicon intellectual property (Si IP) design are also very popular. Communication IC designs and CAD courses are also taught in two schools. In general, these courses have covered the basic requirements for IC designs. What remain to be improved are the quality and the contents of the lecture materials. Another topic to be examined is whether these courses are suitable for the student’s backgrounds in TVE system schools.

The Prototyping & Layout Alliance

As mentioned, six university alliances for promoting the VLSI education programs have been founded and financially supported by the consulting office, MOE in Taiwan. Among them, the “prototyping & layout alliance” targets primarily on the TVE system schools. The P&L alliance is led by two professors, i.e. chair and secretary, from a national university of science & technology. The mission is two-fold, i.e. develop VLSI courses suitable for TVE schools, and sponsor a series of promotion activities such as short courses, workshops and design contests. Currently, there are 43 professors from 17 schools participating in the alliance. Six working committees are formed focusing on specific missions. They are 1) course development 2) seed professor training program 3) FPGA design contest 4) academia-industry collaboration 5) international exchange program and 6) workshop organization. In addition to the MOE, the alliance is also guided by an advisory committee with members mostly from the industry. This is to ensure that the direction of VLSI education reform will meet the expectation from the industry. For the course development, traditionally, TVE graduates working in the IC industry are mostly engaged in the supporting work such as system prototyping & verification, IC layout, and manufacturing level testing. Therefore, in the first phase of the program implementation, the P&L alliance has proposed 4 tracks of courses to help the TVE schools build up their VLSI curriculum. They are 1) FPGA based design and system prototyping 2) IC back end design & layout engineering 3) high speed PCB design and 4) automatic test equipment practices. In the second phase of the program, advanced topics such as system on programmable chip (SOPC) and application specific layout will also be implemented. With the joint efforts of both academia and industry, a new VLSI curriculum and four entry courses, one for each track, were developed. The flowchart of the curriculum is shown in Figure 7 with four course tracks highlighted. The course materials include both power point format lecture/lab notes and video tape demonstration of lab operations. These courses were first pilot run among the allied schools last year. This year, the FPGA and the IC layout courses are further open to all schools. The MOE of Taiwan government also subsidizes these schools to set up the teaching laboratories. Figure 8 shows the number of pilot courses in 4 categories offered by the allied schools in year 2002. Figure 9 shows the number of students took these courses. In total, there are 12 courses offered and 791 students took the courses [3]. The numbers are expected to be higher this year due to the increase in school participation.

Aside from the courses, the alliance also supports many promotion or complementary activities. One of them is to provide training programs for those faculties wishing to transfer to the arena of VLSI education. According to our survey...
results in Table II, the size of faculty in the specialties of semiconductor/process is close to that of VLSI. However, most TVE system schools are unable to purchase expensive semiconductor equipments and thus cannot provide satisfactory research environments. On the contrary, the fundamental research equipments of VLSI design are simply workstations and EDA tools. The formers are becoming cheaper and cheaper due to the advances of computer industry. The latters can be purchased at very low price in Taiwan thanks to the subsidy from the government. As a result, the barrier in setting up the VLSI research environment is much lower than that of semiconductor/process. In addition, hundreds of IC design/testing houses are out there and some of them have been very successful. All these become big incentives to attract people from different majors. In view of this, the training program aims to discover potential manpower and provide them with a smooth transition. This year, the program covers three major topics, i.e. “mixed signal IC layouts”, “FPGA & prototyping” and “backend design flow for cell based design”. It is estimated that ninety people will attend the program. The P&L alliance also provide another seed professor training program. This program is designed for those professors with VLSI specialties but wishing to learn advanced SOC topics and design practices from the industry. Professors attending this program will be sent to an IC design house (company) during the summer for on-site training. The company will assign a mentor engineer to help the visiting professors understand the design flows and practices used in the company. The professors will also be allowed to attend some of the company’s project review meetings and communicate with senior technical staffs. Due to the capacity of the company, only 5 professors will be admitted to the program this year. The alliance will cover their living cost and travel expenses during the visiting. In return, they are asked to compile the industrial experiences and know-how they learn into lecture materials. These materials will be available to the allied schools and hopefully this will help the TVE school teachers in upgrading their teaching quality. The alliance also sponsors various promotion activities such as student design contest, workshop, short course and academia-industry forum. For example, 6 such activities were held last year and 951 people in total attended the events. Financial-wise, the alliance received a total of 284,000 US dollars funding from the MOE in year 2002 [3]. More than 80% of the money were spent in the course development, i.e. FPGA, layout, PCB and ATE. This included the subsidy for schools to purchase new lab instruments and the personnel/miscellaneous spending in compiling the lecture notes. The subsided schools were also required to provide a minimum of 25% matching fund. The expenditure allocation of the alliance funding is illustrated in Figure 10. The funding is increased by about 50% this year thanks to the financial support from the Si-soft project.

OPPORTUNITIES AND CHALLENGES

The VLSI education renovation program has been instantiated in Taiwan for 8 years. The achievements are quite significant. The history of TVE schools joining the program is much shorter. Most of them did not play active roles until past few years. Fortunately, the TVE system schools in Taiwan also underwent some fundamental changes these years. Firstly, many PhD graduates joined the TVE schools due to the rapid PhD program expansion in Taiwan in 90’s. These faculties are young, energetic, and many of them are well trained in the discipline of VLSI, either in IC (integrated circuit) design or process. This has provided a sound basis for the faculty requirement in promoting VLSI education program in TVE schools. Secondly, in addition to hiring more PhD faculties, many private TVE schools have also invested a great deal of money to renovate the facilities in the past few years. Many of them thus passed the evaluations of MOE and were upgraded from junior colleges to institutes of technology, or the universities of science & technology. More students are thus admitted to the schools pursuing higher degrees, i.e. diploma for junior college versus bachelor or master degrees for university. This implies uplift in the education quality of TVE system students. Both factors have paved the way for the promotion of VLSI education program in TVE schools. In addition, the TVE schools have traditionally emphasized on the industry practices in their education. VLSI design happens to be a practical disciple that requires close correlation between the school education and the industry practices. It is therefore very suitable for the development in the TVE schools.

Despite of the promising side, the challenges lying ahead are tough as well. The fundamental one comes from the prejudice of the society in Taiwan. It is deep-rooted in most people’s mind that the TVE system schools are inferior to the regular system schools. Consequently, the TVE system schools often admit less talented students compared with those admitted to the regular system schools. In addition, well trained VLSI majored students, after graduation, often choose to enter a national, regular system university for the graduate program. How to retain good students has become the biggest challenge for the TVE system schools, in particular, the private ones. Another problem to be tackled is to overcome the general impression in industry that TVE system students are less competitive and can only take on supportive works. Fortunately, the situation is changing now. Actually, many TVE graduates are working on the kernel designs due to their solid professional background. Hopefully, with the help of VLSI renovation program, more and more TVE system students can receive better and practical VLSI training so that they become more qualified in their professions. It should be noted that personal characteristics most appreciated by high-tech companies are not confined to professional skills. Personalities such as teamwork, loyalty, and flexibility are also highly valued but not covered in most education programs.
ACKNOWLEDGMENT

The author would like to express his gratitude to the deputy director of the CIC for providing the valuable statistics. Special thanks are also given to those professors responded to the survey.

REFERENCES


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TABLE 1
THE PROFILES OF SCHOOLS RESPONDING TO THE SURVEY

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<th>National</th>
<th>Private</th>
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<td>Univ. of Science &amp; Tech.</td>
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TABLE 2
THE SURVEY RESULTS FROM 11 ALLIED SCHOOLS IN PROTOTYPING & LAYOUT ALLIANCE

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<th>surveyed item</th>
<th>percentage</th>
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<tbody>
<tr>
<td>A.1</td>
<td>Faculty with IC design / EDA specialties</td>
<td>14.2%</td>
<td>in EE/CS departments</td>
</tr>
<tr>
<td>A.2</td>
<td>Faculty with semiconductor process specialties</td>
<td>13.9%</td>
<td>in EE/CS departments</td>
</tr>
<tr>
<td>B.1</td>
<td>Undergraduate students majoring in VLSI</td>
<td>32.5%</td>
<td>Subject to all senior students</td>
</tr>
<tr>
<td>B.2</td>
<td>Undergraduate students entering graduate schools</td>
<td>32.9%</td>
<td>in all majors</td>
</tr>
<tr>
<td>B.3</td>
<td>BS graduates working on IC related jobs</td>
<td>13.1%</td>
<td>subject to all BS graduates, with B.2 excluded</td>
</tr>
<tr>
<td>C.1</td>
<td>Master students majoring in VLSI</td>
<td>30.9%</td>
<td>Subject to all master graduates</td>
</tr>
<tr>
<td>C.2</td>
<td>Master graduates working on VLSI related jobs</td>
<td>22.1%</td>
<td>Subject to all master graduates</td>
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