A NEW SIGNAL DETECTION CARD USING DSP

Hong-De Chang[1], H. T. Wu[2] and Pin-Ming Liu[3]

Abstract — *This paper is aimed at the research and design of a new multi-channel dual-frequency signal detection card to detect 32-channel E1 or 24-channel T1 dual-frequency signals on the ISP system host switches. The card makes full use of the internal peripheral interface and control circuit functions of the Texas Instruments (TI) TMS320C5402 digital communication signal processor. The DSP assembly language takes charge of the HPI, McBSP, DMA and hardware controls of hardware decompression on the DSP hardware interface. Finally, a complete and practical multi-channel dual-frequency signal detection card development and testing module architecture has also been proposed in the paper, and an emulated model card has been completed to emulate Cmd and ST bus signal for detection function verification. All verification work has proceeded at real-time with the DSP system development tools: Code Composer Studio (CCS) and JTAG hardware emulator.*

Index Terms — DTMF detection, ISP , DSP development tools

I. INTRODUCTION

A new multi-channel dual-frequency signal detection card is design to detect 32-channel E1 or 24-channel T1 dual-frequency signals on the ISP system host switches [1]. Data flow on from ISP system host switches is augmented as a result of technological advancement and progress of times. The demand for system performance increases accordingly; hence the KY-1000 [2] dual-frequency signal detection card originally used on host switches is now unable to satisfy current usage needs. Additionally, following TI's introduction of the new generation digital signal processor (DSP), production of TMS320C1x that was used on KY-1000. The price of TMS320C1x still available on the market thus soars. Moreover, slow processing speed (approx. 160μsec.) is the bigger problem of TMS320C1x, it can handle only two channels each time. There is no compatible serial port and microprocessor communication interface; therefore, it is troublesome and time-consuming in circuit design.

As a result, it extensively lowers the overall efficiency of the switch. In short, the old card is not economically efficient and is unable to enhance the overall efficiency of switch. Therefore, the development of a higher performance and more efficient dual-frequency signal detection card to as a replacement for the old one at a low cost-performance value should not be delayed.

The new dual-frequency signal detection card investigated in this thesis should satisfy the following requirements: (1) 32-channel function; (2) programmable communication interface; (3) enhancement of dual-frequency signal decompression and detection abilities; and (4) establishment of the development platform and testing model.

Here is a description of the requirements.

(1) Multi-channel function

ST-bus specification has been adopted to the transfer of digital dual-frequency signals on switch systems; the major frequency at 2MHz provides 32 channels of 8-bit digital dual-frequency signals. The original dual-frequency detection card, available for only 2-channel dual-frequency signal transfer is unable to satisfy performance needs. Therefore, an improvement within the limited hardware of the dual-frequency signal detection card for multi-channels will be an important goal in the circuit design. After careful comparison and consideration, we have chosen the TMS320C5402 DSP [3-4] among the TMS320C54XX series from TI as a solution. With the latest MsBSP technology [5] together with the internal DMA controller, it enables the receipt of dual-frequency signals at 32 channels and a detection of 32-channel dual-frequency signals prior to the next dual-frequency interruption.

(2) Programmable Communication Interface

The architectural differences between the CPU on the old circuit and the host CPU need various buffers and logic circuits to accomplish the command and data transfers between both systems. Hence, to simplify such a complex interface circuit, we apply the HPI (Host Port Interface) technology [5] on the TMS320C5402 DSP to solve software problems.

(3) Enhancement of Dual-Freq. Decompression & Detection Abilities.

Dual-frequency signals are compressed into 8-bit A-law or μ -law PCM code transferred via an ST-Bus on the switch system. Therefore, software has been used to decompress the PCM code after the receipt. If the circuit needs to decompress signals from 32 channels at one time, it not only increases the complexity of the program but also the overhead of the CPU. Hence we have chosen the latest hardware decompression technology provided in the DSP as a solution. Hardware decompression is not only fast and

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efficient, it also reduces the overhead of the CPU, increasing its efficiency. In dual-frequency detection, the high algorithms speed (10μsec) of DSP programmed with the C-language supported software make the algorithms program easier to write and satisfies the requirements for 32 channels.

(4) Establishment of Development Platform and Testing Model

To verify the aforesaid functions, it is necessary to establish a good testing platform and development tools. As shown in Fig.1, we have introduced the Code Composer Studio (CCS) software [7-8] from TI to integrate the development and testing environment as tools for development and test. The ISA type XDS510 hardware interface controller [9] on the PC is connected to the JTAG interface on the DSP to facilitate PC monitoring and DSP execution and buffer contents modification from the PC. Two CCS are hooked on two PCs, one emulates the host card on the switch, another is the multi-channel dual-frequency signal detection card, the ST-Bus cable and command/data cable (Cmd Bus) are connected together independently. In doing so, we can simulate the test on all functions of the multi-channel dual-frequency detection card without a physical switch.

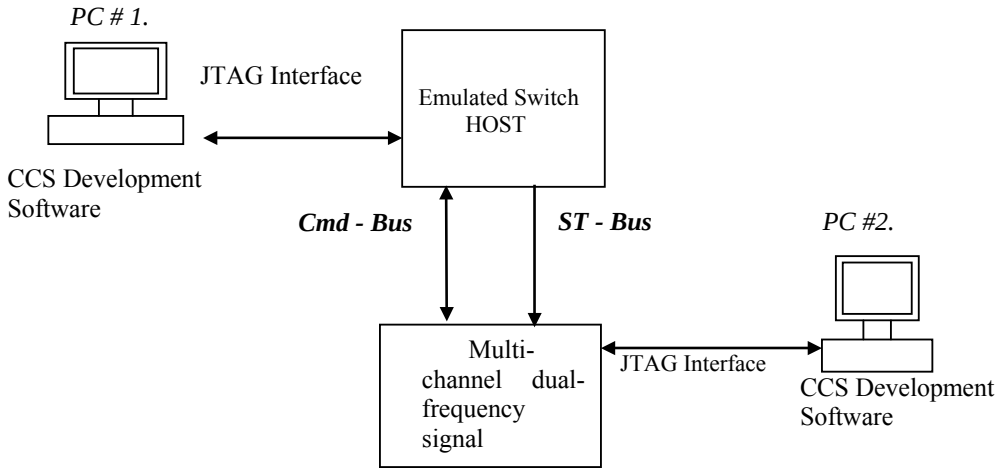

Figure 1 Multi-channel Dual-frequency Signal Detection Development Model

II . ANALYSIS OF DESIGN PRINCIPLES

As shown in Fig. 1, the functions of the switch multi-channel dual-frequency signal detection card fall into three categories: (1) receipt of dual-frequency signal; (2) detection of dual-frequency signal; and (3) transfer of commands and data.

2.1 Dual-frequency Signal Receipt

Dual-frequency signal is transferred to the MFRx from the Host (emulator) via the DMA bus inside the DSP (’C5402) after compressing the 32-channel PCM sample code with the McBSP interface technology through the ST-bus format at 2MHz. MFRx moves the 8-bit PCM code received from the MsBSP Channel 0 to the internal data memory through DMA bus operation and executes Fast Fourier Transform (FFT) conversion algorithms [10] at the DSP before saving the detected dual-frequency signal value to the memory.

McBSP Interface

The interface is a multi-channel buffer serial port [5] that can plan serial data flow transfer specification and speed. The interface planning is applicable to all kinds of industrial data transfer; such as T1, E1 or ST-bus.

DMA Interface

As a data memory access controller, it is designated for transferring and moving DSP internal data and enables circular address setup. It is applicable to fast data sorting to enhance CPU efficiency. It can be used with McBSP inside ’C5402 DPS or inter-memory data movement alone [5].

2.2 Dual-frequency Signal Detection

The dual-frequency signal detection function is at the MFRx, aiming at detecting the value of the present dual-frequency signal and at transferring the value back to the host. The principle overview is shown in Eq.(1), when dual-frequency signals are sampled after quantification at 256 points, divided into even points, physical, (0, 2, 4, 6...256) and odd points, non-physical, (1, 3, 5, 7...255). After FFT conversion, the frequency range response is obtained. Then the strength of signal is compared at different range, and finally the highest and lowest frequencies are obtained. After comparing the value of

various dual-frequency signal groups, the values that match each other are the detected value of the dual-frequency signal.

Formula:

$$X[k] = DFT\{x[n]\}$$
$$= \sum x[n]e^{-j(2\pi/n)kn}, \quad (n = 0 \ldots\ldots\ldots\ldots N-1)$$
$$= x[0]e^{-j0} + x[2]e^{-j(2\pi/n)2k} + \ldots\ldots\ldots + x[N-2]e^{-j(2\pi/n)k(N-2)}$$
$$+ x[1]e^{-j(2\pi/n)k} + x[3]e^{-j(2\pi/n)3k} + \ldots\ldots + x[N-1]e^{-j(2\pi/n)k(N-1)} \quad (1)$$

2.3 Command and Data Transfer

With the HPI technology at MFRx, the host (emulator) writes the 32-channel dual-frequency signal detection commands to the already-planned MFRx data memory with the internal DMA bus and transfers the 32-channel dual-frequency signal values detected at the MFRx back to the host data memory.

HPI-8

It is an enhanced 8-bit HPI to enable two-way communication of data and commands between ’C5402 DSP and any CPU. It also enables handshake, and any CPU can access to data in the DSP internal data memory.

PCM Code Data

Industrial ST-bus standard has been used in PCM code data transfer. 2MHz is the major transfer rate, with the generation of a frame, *A-law or* μ *-law* data at 8-bits/channel from channels 0-31 is transferred on the ST-bus from Bit 7 through Bit 0 (high to low).

Command Format

In detection command transfer, as shown in Table 1, ’00h’, ’01h’, ’02h’ and ’03h’ are used to express Silent or R1, DTMF, R2-Forward and R2-Backward detection of μ -law, respectively. ’80h’, ’81h’, ’82h’ and ’83h’ are used to express R1, DTMF, R2-Forward and R2-Backward detection in A-Law. All these commands are transferred from the HPI-8 on ’C5402 DSP.

III. SYSTEM ARCHITECTURE OF THE SIGNAL DETECTION CARD

3.1 Host Switch System Outline

As shown in Figure 1, the host switch system falls into three sections: (1) client section: main source of dual-frequency signal, mostly from indoor telephones or mobile phones; (2) PSTN: public switching telephone network; (3) ISP systems. The diagram shows the host switch receives dual-frequency signals from PSTN and converts signals required by telecommunication service systems to provide various network service functions for clients. Therefore, the dual-frequency signal detection function of the host switch plays an important role in the entire network. If we fail to enhance it, the service functions of the entire network will be extensively lowered and even unable to achieve the objectives. This thesis therefore aims at the research and manufacture of a switch multi-channel dual-frequency signal detection card to detect at the same time 32-channel E1 or 24-channel T1 dual-frequency signals and at enhancing the dual-frequency signal detection ability of the host switch system to apply to the host switch system on ISP systems.

3.2 Inter-system Data Transfer

The data transfer between the emulated host switch and multi-channel dual-frequency signal detection card, is divided into the emulated host switch (Host) and the multi-channel dual-frequency signal detection card (MFRx). Here is a description of the basic functions:

(1) Host transfers 32-channel dual-frequency detection command code to MFRx through HPI-8.

(2) MFRx transfer the 32-channel dual-frequency detection results back to the host through HPI-8.

As shown in Figure 4, the system composes of two sections, the Host and the MFRx. Here is a description of each section:

3.2.1 Host

It is the center control unit (CCU) of the emulated switch system furnished with two functions: (1) to transfer dual-frequency signals at channels 0-31 to MFRx in PCM code (*A-law or* μ *-law)* via McBSP in ’C5402 DSP; and (2) to transfer dual-frequency signal detection commands at channels 0-31 to MFRx

via HPI-8 in ’C5402 DSP and read dual-frequency signal values detected at MFRx from HPI-8. The main program flowchart shows through McBSP the Host transfer data and waits for Timer1 and DMAC0, when 160 entries of data are transferred from the PCM code at channels 0-31, it means the transfer of data at each channel has been completed. At this moment, PCMadd flag buffer will be set to ‘1’, the Host will call the *GetPCM( )* program to supplement PCM code (160 entries of data/channel) at channels 0-31 to SpeechOut buffer, and will return to main program. Figure 5 is a description of Timer1 and DMAC0 interrupts generated during the transfer.

(1) Timer1 Interrupt

Timer1 interrupts every 0.5 second to read detection values

(channel 0-31) from and write detection commands to MFRx. When Timer1 interrupts, it writes the detection commands of channel 0-31 at CmdBuff address to ExeCmd address at MFRx and transfers values detected at MFRx back to RxCmd address.

(2) DMAC0 Interrupt

To coordinate with the DMA hardware interrupt service program generated by McBSP, DMAC0 (Direct Memory Access Channel 0) interrupts once approx. every 125μsec. When the PCM code data value in the circular buffer set by DMAC0 (at TxBuff, a total of 64 entries) is transferred to half of the buffer via McBSP, it interrupts. It means the PCM code at channels 0-31 has been sent, the Host must supplement such codes to the upper half of the buffer through the SpeechOut address, and when the data value of the buffer has been transferred in full, it interrupts again;

the Host must then supplement the PCM code values to the lower half of the buffer address.

3.2.2 MFRx

MFRx receives PCM code and command code at channels 0-31 from the Host and transfers the detected dual-frequency values back to the Host. It receives PCM codes and command codes from the Host via McBSP and HPI-8, and waits for Timer1 and DMAC0 interrupts. As shown in main program flow in Figure 2, it calls the DetChFreq ( ) program to detect if the PCM code at the present channel contains 160 entries of data. If the quantity is not enough, it moves to the next channel. If the data received is complete, it uses the hardware decompression function (A-law, μ -law) in the 'C5402 DSP to convert the 160 PCM codes to present data values and adds 48 entries of '00h' value to the end of data to form 256 entries of dual-frequency sample values for dual-frequency detection. Finally, it transfers data detected at each channel back to the Host and returns to the main program. Here is a description of the Timer1 and DMAC0 interrupts during the process.

to the memory address of each channel to facilitate dual-frequency signal detection. Timer 1 also blinks LED once every second.

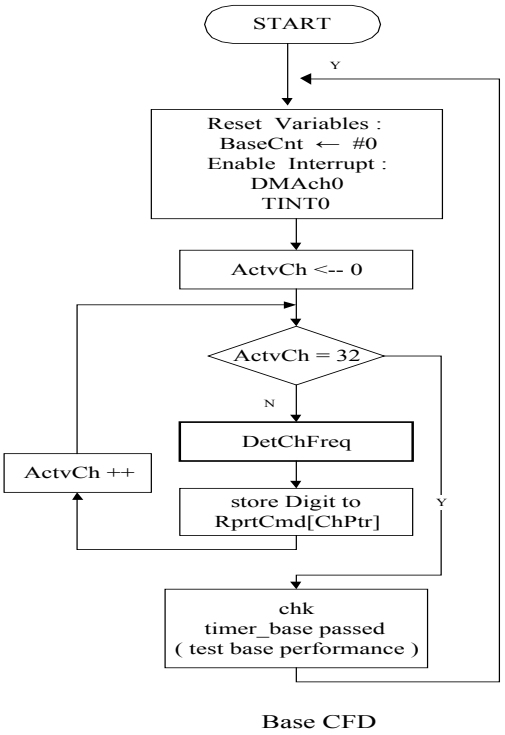

Figure 2 Dual-frequency Detection Signal Flow

3.3 Software Control Data Flow

Data flow also falls into two sections, here is a description.

(A) Host

DMAC0 interrupts once every 125 μ sec, this means the transfer of PCM codes at channels 0-31 has been completed. It is necessary for DMAC0 module program to run PCM code supplementation. Timer1 makes command and data value access to MFRx every 0.5sec, it is accomplished by Timer1 module.

(B) MFRx

DMAC0 also interrupts once every 125 μ sec, it means it has received in full PCM code data at channels 0-31 transferred from the Host. At this moment, it will put data of channels 0-31

3.4 Software Interrupt Level

The interrupt level at both the Host and MFRx is the same, the priority of interrupt is decided by the DMAC0 interrupt to prevent data loss of PCM code at channels 0-31 as a result of improper interrupt and finally to cause inability to perform dual-frequency signal detection.

IV. TEST RESULTS

4.1 Solution to problems in practice

The problems fall into hardware and software aspects.

A. Software Test

(1). Algorithms

To verify the accuracy of DFT algorithms, it is necessary to load physical dual-frequency data, though it was not available in real-time in the software test. As a solution we generated dual-frequency signals as samples with signal generation software to replace physical hardware signal to complete the algorithm verification.

(2). Logic and Control

Software verification logic and control include C and Assemble functions call, hardware DSP buffer setup, *A-law* and μ *-law* processing and verification.

B. Hardware Test

(1). Hardware

No direct communication with the switch system was available during hardware testing. In order to ensure the integrity of tests during R&D, we also designed a Host hardware to emulate a physical switch during the manufacture of the dual-frequency card. Some circuit design errors have deprived the hardware from normal operation during the tests, however normal operation was attained after frequent modification and addition of logic circuit control.

(2). Signal Communication

Signal communication was originally done by two DSPs, one as MFRX, and another as host (switch emulator). In order to ensure switch system integrity, we have replaced the emulated host signal with a dual-

frequency signal generated by a physical switch system in the test.

4.2 DTMF Test

The high-speed calculation ability of 'C5402 DSP enables dual-frequency signal at each channel to be accurately decompressed into linear data from PCM code by hardware decompression and to complete the algorithms within the default time and order. In addition, the use of the excellent interface technology reduces the delay effect and system overhead caused by complex circuitry. Hence, the test results satisfy the anticipated conceptions, and the function of switch system is thus diversified and the overall performance is enhanced. Here is a description of the testing results with two sets of dual-frequency signals, DTMF_1 of μ ***-law*** and DTMF_1 of ***A-law***, in terms of a time domain chart and frequency domain chart.

A. Test on DTMF_1 of μ ***-law***

As shown in Figure 3, we put the 160 entries of μ -law DTMF_1 PCM code samples in memory at address 0140h - 01dfh. After hardware decompression, they are put at address 3030h for DFT conversion and detection of dual-frequency value. Figure 4 shows the 160 entries of linear data at 3030h expressed in a time domain chart, where the time domain signal is formed by two signals, one at a higher frequency (1336Hz) and the other one at a lower frequency (697Hz). After DFT calculation, the data are expressed in a frequency domain chart as shown in Figure 5. It is clear that the dual-frequency signal is composed by two types of frequencies, low frequency at 697Hz, high frequency at 1336Hz. Then we can see the dual-frequency signal is DTMF_1.

B. Test on DTMF_1 of ***A-law***

In addition, we put the received 160 entries of A-law DTMF_1 PCM code samples in memory at address 01e0h – 027fh. After hardware decompression, they are put at address 3030h for DFT conversion and detection of dual-frequency value. It can also be shown that the 160 entries of linear data at 3030h expressed in a time domain chart, and the time domain signal is formed by two signals, one at a higher frequency (1336Hz) and one at a lower frequency (697Hz). Then we can also see the dual-frequency signal is DTMF_1.

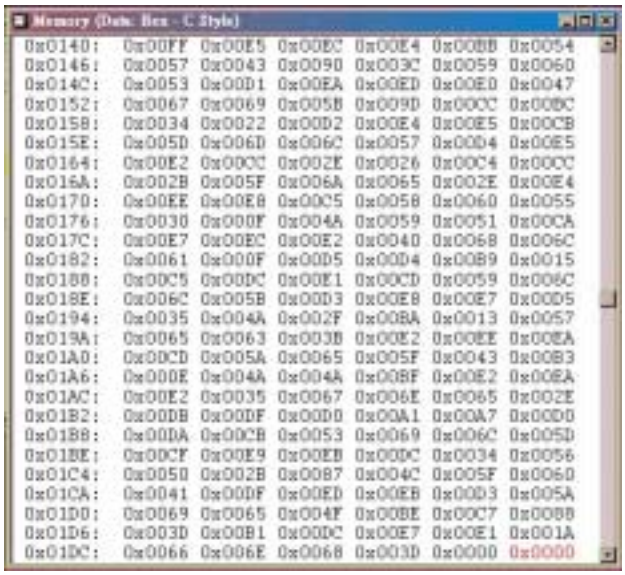

Figure 3 μ *-law* PCM code Sample

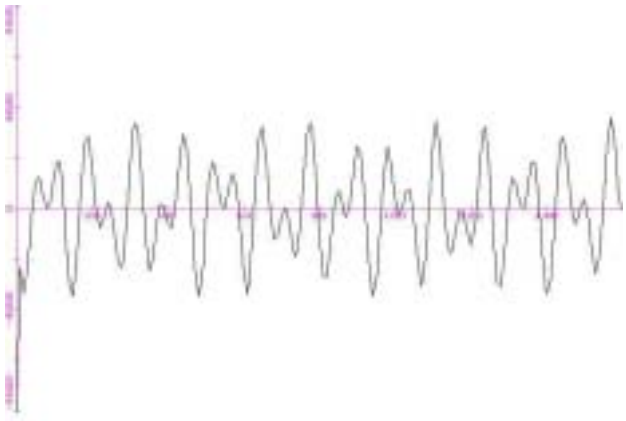

Figure 4 Time Domain Chart

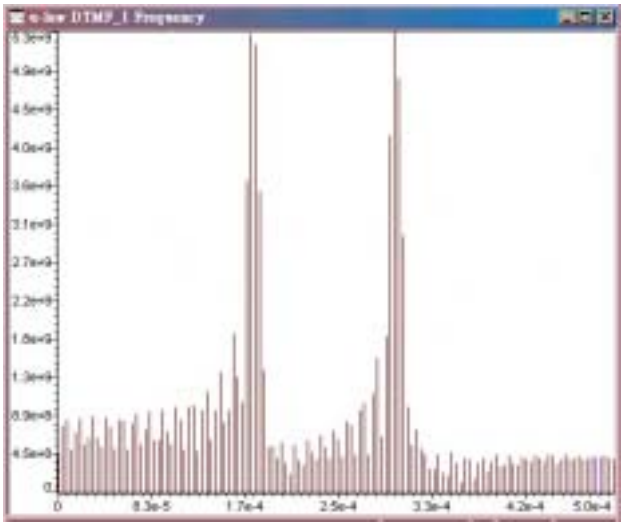

Figure 5 Frequency Domain Chart

V. CONCLUSION

A comparison of the old and new dual-frequency signal detection cards is addressed. In memory size, the old card has RAM (144 byte) and ROM (1.5 k), which are smaller than the 16K and 4K of the new card, respectively. In external program and data memory addressing, the old card can only address program memory to 4K, and it is unable to address data memory. The new card can address to 1M and 64K. In parallel port, only 8*16 bit interface is available on the old card, while there is HPI on the new card. Serial port is unavailable on the old card, while there is a McBSP on the new card. There is no DMA controller on the old card, and there are DMA controllers for 6 channels on the new card. There is no timer on the old card, while there are two on the new card. In processing speed, the instruction cycle time on the old card is 160n sec, while it is 10n sec on the new card. In packaging, the old card is available in two options: DIP and PLCC; the new card has BGA and TQFP. In dual-frequency signal detection function, the old card can detect only 2 channels at a time, while the new card can detect 32 at a time. The production cost of the old card is also higher. As a conclusion, the features, the speed, the memory size and the price of the new card are much better than the old one, and it can enhance the system efficiency and reduce production costs.

Consequently, dual-frequency signal is widely apply to telecommunication, they are different only in their specifications. For examples, DTMF, R1, R2, they are different because of the composition. The protocol is different according to the system used in different countries, such as T1, E1, Cable Modem or ST-BUS. The multi-channel dual-frequency signal detection card completed in this research is based on the ST-Bus transfer standards and *A-law*, μ *-law* decompression methods to provide 32-channel (0-31) dual-frequency signal detection. The new multi-channel dual-frequency signal detection card is an overall improvement in switch system performance. Here are the advantages:

(1) To detect figure data of 32-channel handset at the same time.

(2) Adjustable to *A-law* or μ *-law* decompression according local system.

(3) Expandable to 64 or 128 channels according the needs of switch system.

The information technology advancement pushes the progress in switch systems. Switching systems thereafter will combine radio communication, LAN, Internet, remote control and all kinds of modern functions. In the future, we will continue or R&D on all kinds of multi-channel dual-frequency signal detection cards in order to satisfy the needs of various switching systems.

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