Building Up A Multi-Core Educational Environment in Taiwan

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Abstract

For promoting the research and education of multi-core embedded systems and applications, a national program, named the Multi-Core Educational Environment Deployment Program, was carried out by CIC and supported by National Science Council of Taiwan. In this paper, the objectives, practice procedures, and preliminary achievements for building up the researching and educational environment of multi-core embedded systems in Taiwan are presented.

1. Introduction

National Chip Implementation Center (CIC) has been serving the academic and industrial societies in Taiwan for more than 15 years. The main objective of CIC is to provide highly qualified IP design and implementation services to the academia of Taiwan. We continuously introduce advanced IC/system design technology to the campus, provide design environment, assist professors and students to implement their innovative works, and play the role as a bridge between academic and industrial societies.

For promoting the research and education of multi-core embedded systems and applications, a national program, named The Multi-Core Educational Environment Deployment Program, was carried out by CIC and supported by National Science Council of Taiwan. In the rest of paper, the main objectives of the program are explained in Section 2; the practice procedure is described in Section 3; the preliminary achievements and statics are presented in Section 4; we finally state the conclusion in Section 5.

2. The Main Objectives

In accordance with the procedure of our previous program[1], CIC had to build an universal study platform as an information center and a database. Vendors and research members from campus exchanged resources and experiences via the CIC universal study platform. We had to complete three main objectives as follows:

- **Evaluating and procuring multi-core embedded platforms**: CIC decided the procurement specification of multi-core embedded hardware platforms by surveying recent technologies and collecting demands from academia. In this program, we introduced five multi-core embedded processor designs and their respective hardware evaluation kits. We also set up and tested these kits, searched available software development solutions, and created quick-start manuals.
- **Deploying multi-core embedded platforms and establishing research environments**: The majority of the procured kits were provided to laboratories in campus planning or proceeding to research multi-core related technologies. The rest kits were used for setting up the training classroom in CIC. We also provided technical consultation and FAQ lists for the users. Only advanced technical questions or additional requirements were passed to the vendors (manufacturers or agents) of these evaluation kits. By this service model, the service latency to users was reduced, and the providers could focus on solving key issues.

- **Offering reference design and providing training courses**: Several reference designs were created by CIC or collected from vendors. With open-sourced reference designs, students do not have to blindly spend much time searching for design samples, and transparent source codes further help students understand details of design concepts. Otherwise, the respective courses of these adopted multi-core evaluation kits were delivered in CIC to shorten the learning time to students for handling boards and software tools.

3. The Practice Procedure

For fairly allocating the resources and arousing novel research topics, professors who intended to participate in this program had to submit a proposal to CIC. The research subject, target platform, progress schedule, and estimation of difficulities should be well described in the proposol. A committee formed by CIC decided the acceptance of these proposals by their originality and fesibility. Applicants were not restriced to request one platform. The multi-core embedded hardware platforms dopted by CIC are described here:

A. ITRI PAC Duo

PAC (Parallel Architecture Core) is a high performance and low energy cost DSP developed by ITRI (Industrial Technology Research Institute of Taiwan). PAC Duo is a heterogeneous tri-core hardware platform designed mainly for multimedia and parallel applications. Two domestic 5-way and 9-stage VLIW DSPs are connected by an AXI bus and another ARM926EJ-S processor on an AHB bus is for controlling and general purpose computation. The PAC Duo evaluation board includes DDR2 controller, Ethernet controller, and plenty of other peripherals. The software tool chain is also complete. The structure of PAC Duo is shown in Figure 2.

B. ANDES ADP-AG102

The ANDES ADP-AG102 is another domestic design in Taiwan. It consists of two 32-bit and 5-stage pipeline processors, supporting 16/32-bit mixed instruction set. The maximum working frequency of the core can reach 533 MHz. The architecture of ANDES ADP-AG102 is as shown in Figure 3. ANDES also provides a well-integrated software debugging IDE along with a Linux kernel to the evaluation board.

C. Digilent XUPV5-LX110T

The Digilent XUPV5-LX110T [2] itself is a low-cost, versatile evaluation board often adopted by a FPGA course. We chose this broad for evaluating the Sun (now part of Oracle) OpenSPARC T1 processor design. OpenSPARC T1 is a high-performance chip-level multithreading design, and the number of cores in an OpenSPARC T1 processor can be flexibly configured. The OpenSPARC project is open-sourced; all of the source code, documents, bit-file, and toolchain, are available in [3].

D. Virtex-5 FXT ML510 Embedded Development Platform

The Virtex-5 FXT ML510 [4] integrates dual PowerPC440 processors, a PCI Express bus, and other high speed peripherals on its FPGA. The cross-compiling toolchain for PowerPC 440 can be found on Internet.

E. Cell Processor Development Platform

The Cell processor is a well-know heterogeneous multi-core processor design in recent years. Its high speed Element Interconnect Bus along with the Power Processor Element and Synergistic Processing Elements provide tremendous computing power. The Cell Processor Development Platform is actually a PlayStation 3 game console with the Fedora Linux and Cell SDK installed inside [5]. This configuration had already been adopted by [6] and other multi-core programming courses.

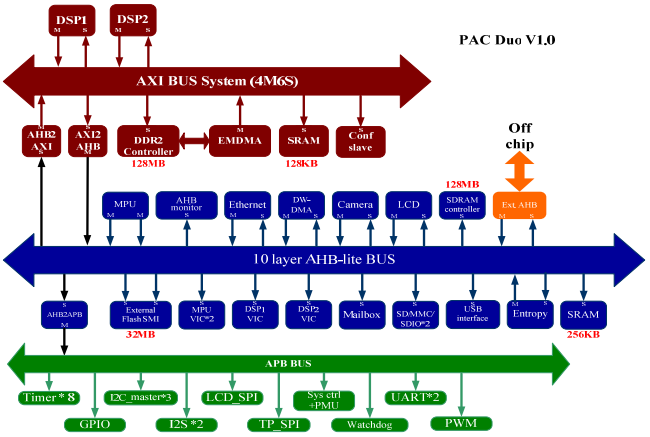

Figure 1: The Architecture of ITRI PAC Duo

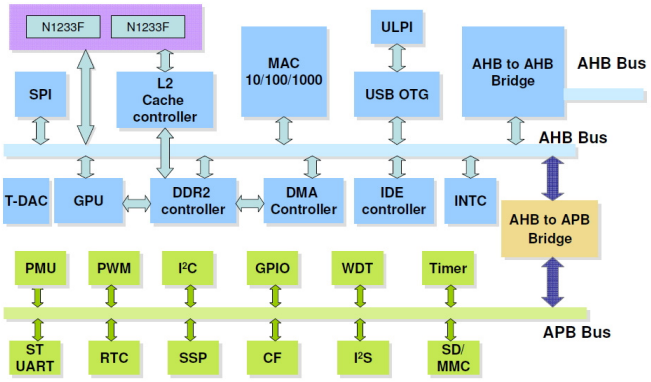

Figure 2: The Architecture of ANDES ADP-AG-102

CIC also introduced system-level simulation tools and processor/peripheral IPs for ITRI PAC, ANDES and PowerPC platforms, thus users who selected these platforms could go though a complete design flow and further implement their designs to real SoC systems.

4. Preliminary Achievements

During the first year of the program, CIC held nine courses for the five multi-core evaluation kits and their related tools, 364 professors and students attended these courses. CIC finally accepted 65 proposals from 46 professors in 31 universities. Two reference designs were created by CIC and another two designs are provided by vendors. Since the procurement of kits took time and so did the learning steps by students, most of these researches are still in early stages. However, we have received feedback information from the users.

The Figure 3 illustrates the proportion of each platform among all applications. Although the Cell platform lacks flexibility by its ready-made PS3 hardware, it is still favorable because of its high performance and the powerful SDK. The ITRI PAC Duo platform is also favorable due to its high accomplishment of hardware and software solutions, even including a H.264 decoder reference designs; the domestic support from ITRI is also advantageous for reducing the difficulties during the learning period. The Figure 4 reveals the proportion of research topics among all proposals. The categorization is rough since many topics have multiple attributes. The developments of multimedia algorithms and systems formed the majority of the proportion. This phenomenon is not extraordinary since most of the multi-core processor designs are on purpose of multimedia applications. The scientific/engineering computation topics are relatively rare and most of their intentions are developing signal processing algorithms. The possible reason is that handling embedded systems needs extra efforts to familiar hardware and firmware configurations. Researchers doing basic scientific researches may prefer to perform their works on computer-based systems.

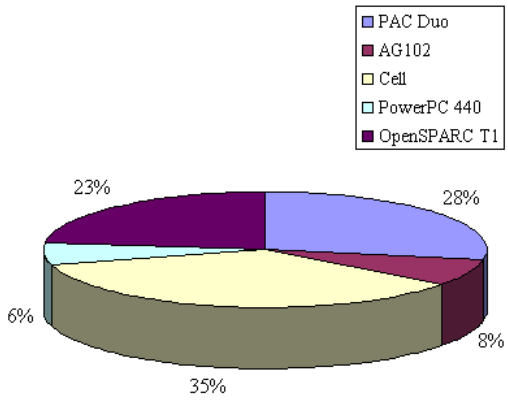

Figure 3: Proportion of applied platforms

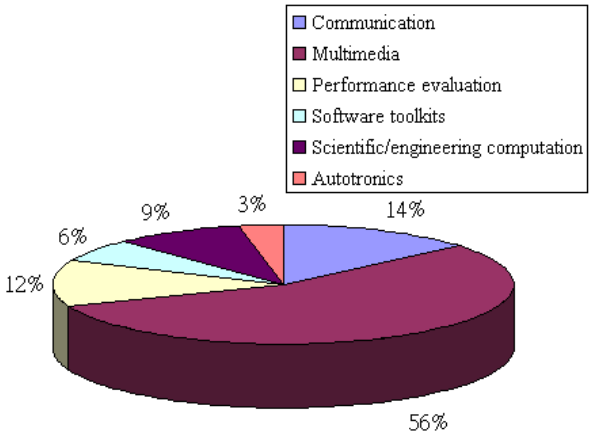

Figure 4: Proportion of research topics

5. Conclusions

As all of the missions and objectives achieved by CIC, we will continuously fulfill the demand of multi-core related system researches from the academia of Taiwan. Our further work is to strengthen the functionality of the universal study platform. Sharing experiences among users, vendors and CIC will be greatly useful to leap over the threshold of learning multi-core system design techniques.

References

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