Teaching and Design on Integrating Interpolation Electronics for Nanometer Measurement and Positioning

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Abstract *— This paper presents a method, to teach the senior students how to integrate the multi-domain knowledge of electronics, optics, control as well as precision measurement, and proposing a high resolution subdividing electronics module to the sinusoidal encoder output of positioning motor, such that the module can not only be used as a counter for linear and/or angular measurements, but also subdivide the periods of the sinusoidal encoder signals up to 1600 times. Firstly, for making digital noise filter, digital frequency multiplier and counter, we use M4A5-64/32 which is a Complex Programmable Logic Device (CPLD). Then, for counting the quadrature-signals with 90 degrees of phase difference, it is required to make the two waves with the same amplitude as well as DC offset. So, they can be represented as signals of cosine and sine. Using these two signals one can get the arctangent (ATAN) value of which, and then the corresponding phase angle is obtained by interpolating the waves within a single period. Finally, is to convert the phase angle into displacement. Secondly the mechanism for test is briefed, including stepping motor and its driver module, Linear Variable Differential Transformer (LVDT) and its signal processing module, optical encoder, as well as the digital circuit with high speed 8051 microprocessor. In which the sinusoidal encoder and laser interferometer are frequently used for nanometer position control. At last, the purpose of laser interferometer and its operation principle are illustrated. From the results of experiment test it can be seen that the whole module is suitable for those applications requiring high-resolution encoder, nanometer measurement as well as fast data acquisition with phase tolerance of ± 45 degrees.*

Index Terms *— Subdividing, Interpolation, Angle Encoder with Sinusoidal Voltage Output, Linear Scale, Quadrature-Phase Interferometer, Precise Positioning*

INTRODUCTION

The trend in production industry towards higher throughput along with the requirement of improved quality leads to an increasing demand for nanometer measurements and positioning. However, dimensional measurements and motion positioning from about several nanometers to tens of meters are most important. Because the measurements of mechanical tools, industrial products, scientific research and many dimension related fields, such as flatness, and roughness, etc., are almost all in this field. So that for the students to familiar with the metrology field, precise and nanometer measurement is the first step of learning.

This paper presents a method, to teach the senior students how to integrate the multi-domain knowledge of electronics, optics, control as well as precision measurement, and proposing a high resolution subdividing electronics module to the sinusoidal encoder output of positioning motor, such that the module can not only be used as a counter for linear and/or angular measurements, but also subdivide the periods of the sinusoidal encoder signals up to 1600 times. In which a prototype of interpolation module is developed by using quadrature-phase interferometer and sinusoidal encoder. The analog to digital converter (ADC) and complex programmable logic devices are used to develop this quadrature-signal interpolation for high-precision and cost-efficient consideration.

Firstly, the most important role on the interpolation electronics design is portrayed for the students, including complex programmable logic device (CPLD), digital noise filter, digital frequency multiplier and the whole interpolation circuit. Lots of logic devices are housed in one CPLD. Those connections can be specified using the development program. The function of the CPLD device can be made by using the development languages such as VHDL, Verilog, and ABEL, or by the way of graphic editing. CPLD is convenient that it is possible to rewrite many times, because the contents of the circuit are recorded to the flash memory. CPLD with In-System Programmability (ISP) can help accelerate development time, facilitate in-field upgrades, simplify the manufacturing flow, lower inventory costs, and improve printed circuit board (PCB) testing capabilities.

For digital noise filter, digital frequency multiplier and counter, we use M4A5-64/32 CPLD, which manufactured by Lattice®. For interpolation main function, we use EP1K30 CPLD, which is been categorized to Field Programmable Gate Arrays (FPGA) by Altera®. For counting the quadrature-signals with 90 degrees of phase difference, normally, the requirement is that the two waves have the same amplitude as well as DC offset. So, they can be represented as signals of cosine and sine. Using these two signals we can get the arctangent (ATAN) value, the corresponding phase angle will also be obtained when we interpolate the waves within a single period. Finally, we can convert the phase angle into displacement.

But for the variation of actual quadrature-signals, they are not always satisfying these required terms. Such as quadrature-laser interferometer, amplitude and DC offset voltage of output signal will be influenced by laser intensity and measuring distance. With the result, the amplitude and DC offset voltage will be variable. Also the phase difference of these two signals will be changed by the variance of laser polarization, and not always be 90 degrees. All of these parameters will affect the accuracy of displacement measurement.

Secondly we briefly describe the mechanism of test in the course, including stepping motor and its driver module, Linear Variable Differential Transformer (LVDT) and its signal processing module, optical encoder, as well as the digital circuit with high speed 8051 microprocessor. In which the sinusoidal encoder and laser interferometer are frequently used for nanometer position control. At last, the purpose of laser interferometer and its operation principle are illustrated. From the results of experiment test it can be seen that the whole module is suitable for those applications requiring high-resolution encoder, nanometer measurement as well as fast data acquisition with phase tolerance of ± 45 degrees.

PRINCIPLES OF OPERATION

In this section, we make some descriptions used in the experiments and verification for the students. The signal flow chart of the whole interpolation circuit is shown in Figure 1. Not only can we process counting of cycle number by three functions: square wave conversion, direction detection, and counting of cycles, but also process normalization, conversion of corresponding degree, degree variance conversion within every single cycle.

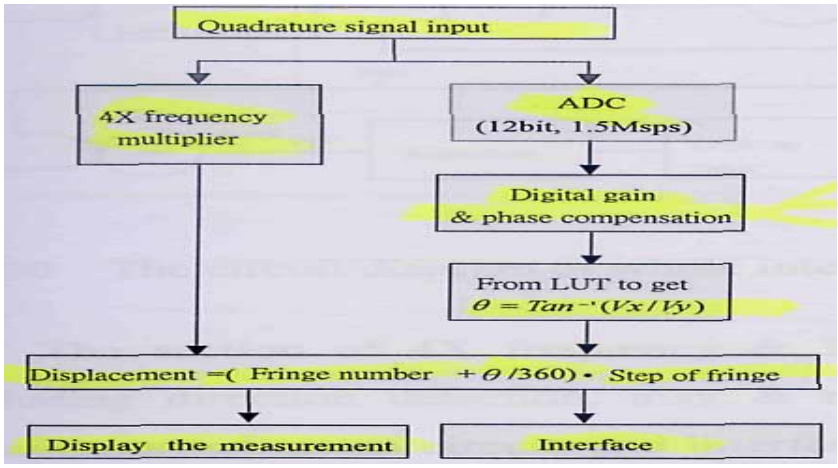


FIGURE 1
THE SIGNAL FLOW CHART OF WHOLE INTERPOLATION CIRCUIT

Introduction for CPLD Application: The interpolation function will be evident from the circuit block diagram of Figure 2 illustrated below. From Figures 1 and 2 we can see that the most important components in the interpolation electronics design are complex programmable logic device (CPLD), digital noise filter, digital frequency multiplier, and the whole interpolation circuit. Lots of logic devices are housed in one CPLD. Those connections can be specified using the development program. The function of the CPLD device can be made by using the development languages such as VHDL, Verilog, and ABEL, or by the way of graphic editing. CPLD is convenient that it is possible to rewrite many times, because the contents of the circuit are recorded to the flash memory. CPLD with In-System Programmability (ISP) can help accelerate development time, facilitate in-field upgrades, simplify the manufacturing flow, lower inventory costs, and improve printed circuit board (PCB) testing capabilities.

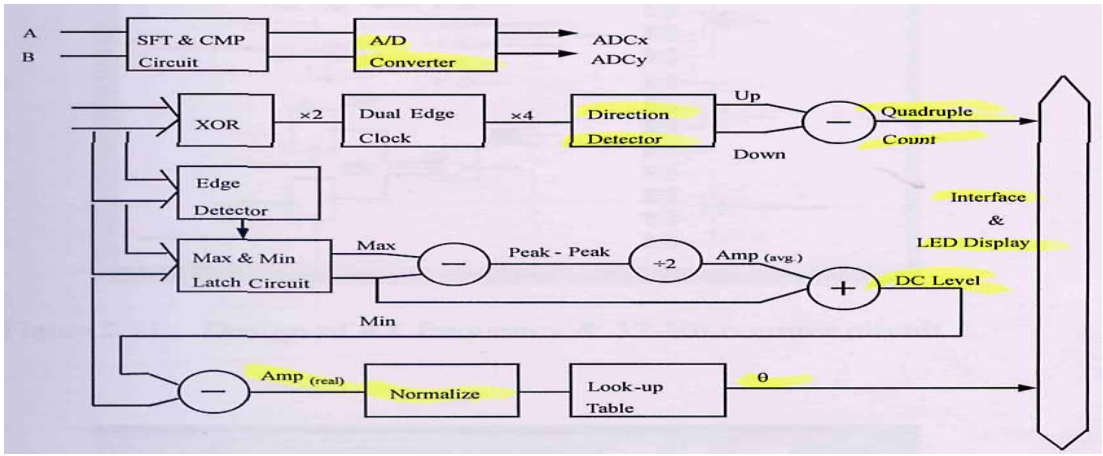


FIGURE 2
THE CIRCUIT BLOCK DIAGRAM OF THE INTERPOLATION FUNCTION.

For digital noise filter, digital frequency multiplier and counter, we use M4A5-64/32 CPLD [6]. For interpolation main function, we use EP1K30 CPLD [7], which is been categorized to Field Programmable Gate Arrays (FPGA). All the developments of CPLD are using graphic editing. Figure 3 shows a schematic example.

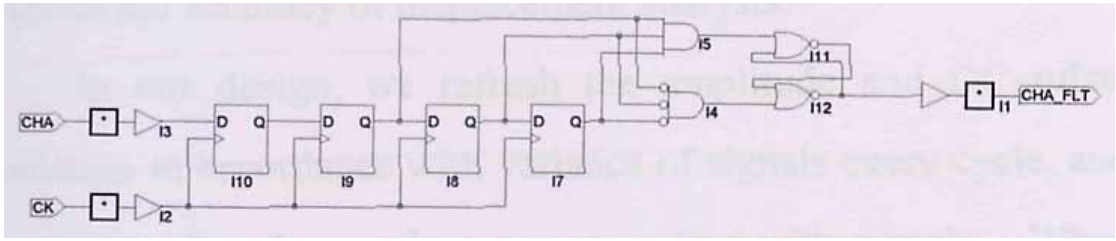


FIGURE 3
DESIGNING CIRCUIT BY USING GRAPHIC EDITOR

For the students, CPLD with in-system programmability (ISP) can help accelerate development time, facilitate in-field upgrades, simplify the manufacturing flow, lower inventory costs, and improve printed circuit board (PCB) testing capabilities. As PCBs become more complex, the need for through testing becomes increasingly important. Advances in surface-mount packaging and PCB manufacturing have resulted in smaller boards, making traditional test methods--e.g., external test probes and "bed-of -nails" test fixtures-harder to implement. As a result, cost savings from PCB space reductions are sometimes offset by cost increases in traditional testing methods [5]. The CPLD device can write data on the personal computer to the CPLD device with the JTAG protocol specified by IEEE1149.1 (JTAG Boundary Scan). This interface allows devices to be programmed and the PCB to be functionally tested in a single manufacturing step, saving testing time and assembly cost. The experimental setup shows in Figure 4.

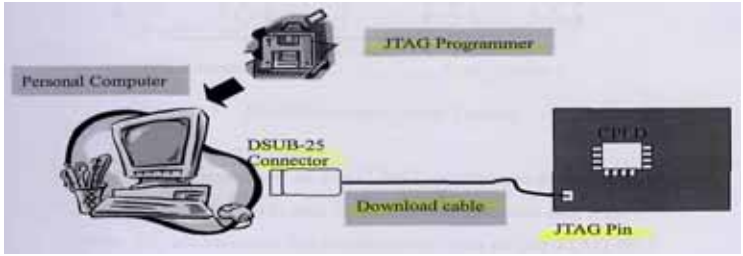


FIGURE 4
DOWNLOAD JTAG FILE FROM PC TO CPLD.

Boundary-Scan Test (BST) Architecture: The boundary-scan test (BST) architecture offers the capability to efficiently test components on PCBs with tight lead spacing. The students can use the BST architecture to test pin connections without using physical test probes and to capture functional data while a device is operating normally. Boundary-scan cells in a device can force signals onto pins, or capture data from pin or core logic signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared to expected results. Figure 5 illustrates the concept of boundary-scan testing.

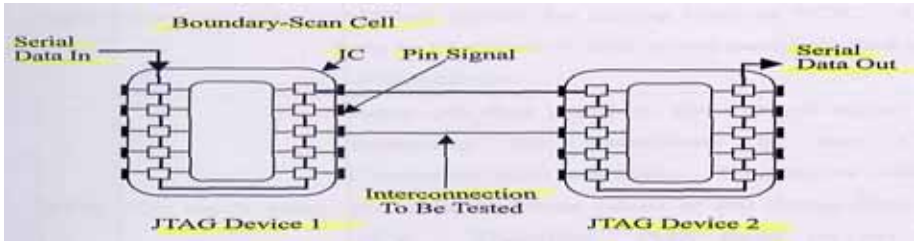


FIGURE 5
ARCHITECTURE OF JTAG BOUNDARY-SCAN TESTING

Interpolation Circuit Design: This section teaches the students how to count the signals in quadrature. Normally, most condition assuming that the two waves have 90 degrees difference, and their amplitude as well as DC offset must be the same. So, they can be represented cosine and sinusoidal signal. We sub-divide these sinusoidal signal and cosine signal, then we get the ATAN value, the corresponding phase angle will also be gotten when we interpolate the waves within single period. And we can convert the phase angle into displacement. But for the variation of actual signals, they are not always satisfying these required terms. Such as the quadrature-laser interferometer, amplitude and DC offset voltage of output signal will be influenced by laser intensity and measuring distance. With the result, the amplitude and DC offset voltage will be variable. Also the phase difference of these two signals will be changed by the variance of polarization of laser, and not always be 90 degrees. All of these parameters will affect the accuracy of displacement analysis. In our design, we refresh the amplitude and DC offset voltage in accordance with variance of signals every cycle, and we normalize these values corresponding with signals. When we want to get the result of subtle interpolation, we will pay attention to the influence of phase difference. When we proceeding with interpolation in every single cycle, we can get the phase angle within this cycle after our normalized the signal. By this way, we can get the correspondent allocation of signal in this single cycle. While the phase difference is between 45 degrees to 135 degrees, this method is suitable for applications. We have to take notice of the two corresponding value handle with division, the divisor can not be zero. This situation will not happen in our design due to our using COS^{-1} function to calculate the degree.

Further, the sinusoidal signals only have tiny variances in the wave crest and wave trough. And the variance of slope is also tiny. The sensitivity is also not so good for sensing the difference there. However, we not only can calculate the sinusoidal signal A but also can calculate sinusoidal signal B in our design for displacement variance. And these two calculated value will be equal but their sensitivity may be different. It doesn't matter. User can choose the better sinusoidal signal, which lower noise or higher amplitude, or both of them for processing. By this way, the user can get the better accuracy of signal interpolation in every single cycle.

Design of Digital Noise Filter: This section teaches the students what is the principle of digital noise filter to reject noise on the incoming quadrature-signals. The input section uses two techniques to implement improved noise rejection. Schmitt-trigger inputs and a two-clock-cycle delay filter combine to reject low level noise, and large but short duration noise spikes that typically occur in motor system applications. Both common mode and differential mode noise are rejected. The user benefits from these techniques by improved data in the counter. False counting triggered by noise can be avoided. Figure 6 shows the schematic of the input section. The signals are first passed through a Schmitt trigger buffer to address the problem of input signals with slow rise times and low level noise (approximately < 1V). The cleaned up signals are then passed to a 2-bit delay filter. The signals on each channel are sampled on rising clock edges. A time history of the signals is stored in the 2-bit shift registers. Any change on the input is tested for a stable level being present for three consecutive rising clock edges. Therefore, the filtered output waveforms can change only after an input level has the same value for one consecutive rising clock edges.

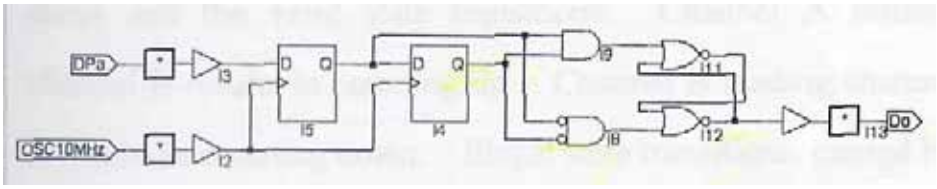
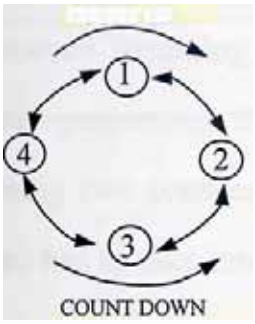


FIGURE 6
DESIGN OF DIGITAL NOISE FILTER

Quadrature Decoder: The quadrature decoder decodes the incoming filtered signals into count information. This circuitry multiplies the resolution of the input signals by a factor of four (4X decoding). When using an encoder for motion sensing, the user benefits from the increased resolution by being able to provide better system control. The quadrature decoder samples the outputs of the PA and PB filters. Based on the past binary state of the two signals and the present state, it outputs a count signal and direction signal to the internal position counter. On the following Figure 7, we illustrate the quadrature states, the valid state transitions as well as the timing diagram. Channel A leading channel B results in counting up. Channel B leading channel A results in counting down. Illegal state transitions, caused by faulty encoders or noise severe enough to pass through the filter, will produce an erroneous count.



CHA	CHB	STATE
CLK STATE	0	1
1	1	2
0	1	3
0	0	4

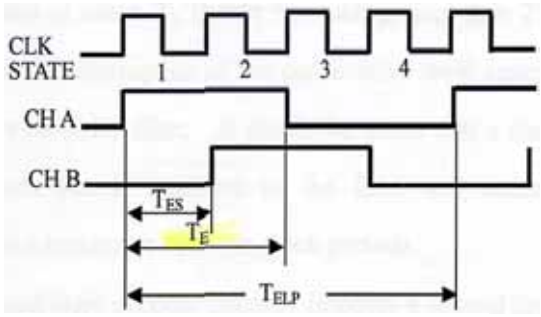


FIGURE 7
PICTURE OF QUADRATURE STATE TRANSITION AND TIMING DIAGRAM.

Interpolation Circuit: Our counting method is for measuring the corresponding allocation variance of two signals, which their amplitudes and DC offset voltages can be different. Even the phase difference can be varied, not always 90 degrees. The design is suitable for sinusoidal encoder and laser interferometer. The two signals can be described as [9]

$$Vx = j + a\cos(\theta) \quad (1)$$

$$Vy = k + b\cos(\theta - \varphi) \quad (2)$$

Where *j and k* are the DC offset voltages of two signals, *a* and *b* are the ac amplitudes of two signals, θ is the phase of signal, and the φ is the phase difference of two signals.

By conditioning circuit of which we will describe later, the DC offset voltage can be eliminated, and we can get the two signals simplified as

$$Vx = 2a\cos(\theta) \quad (3)$$

and $$Vy = 2b\cos(\theta - \varphi) \quad (4)$$

After the shift conditioning circuit to get (3) and (.4), we use analog-to-digital converter (ADC) to get the discrete-time signal value. For considering the maximum input frequency and resolution, we chose AD9221 which is manufactured by Analog Devices®. The AD9221 [10], is a generation of high performance, single supply 12-bit analog-to-digital converter. This device exhibits true 12-bit linearity and temperature drift performance as well as 11.5 bit or better ac performance. This device is a complete, monolithic ADC with an on-chip, high performance, low noise sample-and hold amplifier and programmable voltage reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application. Then, we can proceed with counting of cycle number and signal interpolation within every single cycle. The signal flow chart and the function block diagram of whole interpolation circuit are illustrated in Figures 1 and 2. Not only we can process counting of cycle number by three functions: square wave conversion, direction detection, and counting of cycles, but also process normalization, conversion of corresponding degree, degree variance conversion within every single cycle.

Stepping-Motor and Its Driving Method: Rotary stepping motor is one kind of electric machinery, which can accept digital control signals. In other words, every one input digital pulse signal (or step) will result from one step angle in stepping motor rotation. It is well known that pulses number is direct proportioned to rotation angle of rotary stepping motor. So, it can be easily control by the way of open-loop method. Mainly, there are three magnetic excitation methods for the stator of stepping motor: 1-phase, 2-phase, and 1-2 phase magnetic excitations. What is called that 1-phase and 2-phase magnetic excitations, are simultaneously only one set of core, and two sets of core be excited, respectively. And the method of 1-2 phase magnetic excitation is the 1-phase and 2-phase excitations being exchanged over and over again. In our test equipment, we use one kind of more precise. Briefly, this precise micro-stepping method using electrical circuit to divide one step to divided tiny steps by the way of controlling current of 2-phase.

Mechanism for Testing Rotary Encoder and LVDT: We use rotary encoder and LVDT for testing the interpolation circuits by using one kind of scanner which driving stepping motor. Figure 8 shows the picture of this test mechanism.

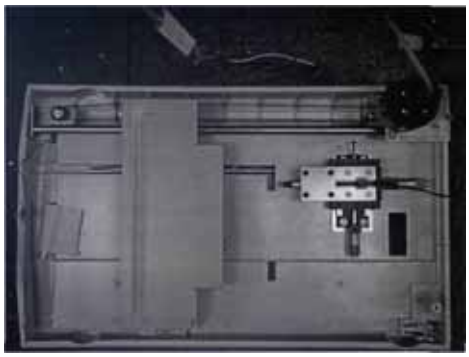


FIGURE 8
MECHANISMS FOR TESTING THE INTERPOLATION CIRCUITS BY USING ROTARY ENCODER AND LVDT.

LVDT and Its Signal Processing: The Linear Variable Differential Transformer (LVDT) is one of the most common mutual inductance elements. It produces an electrical output corresponding to the displacement of a separate movable core. AC carrier excitation is applied to the primary. Two identical secondary coils, symmetrically spaced from the primary, are mostly connected externally in a series-opposing circuit. When the non-contacting magnetic core is displaced from the null position, an electromagnetic imbalance occurs. This imbalance generates a differential AC output voltage across the secondary-coils which is linearly proportional to the direction and magnitude of the displacement. A balanced demodulator can transform this variable ac output into a bipolar dc output that, when referred to the LVDT reference, or null, position, indicates the displacement [11]. The circuit block diagram for LVDT along with a commutating modulation / demodulation circuit for signal processing signal conditioning are shown in Figure 9. The excitation signal is a I Vrms, 1KHz carrier. The low pass filter at right, with a 10 Hz corner frequency, can remove high frequency noise. The amplitude stability is critical because the voltage level of the carrier signal applied to an LVDT or an ac bridge directly affects the overall system sensitivity. Therefore, the carrier amplitude must be stable against loading, time, supply voltage and temperature changes. Waveform purity is also important. High harmonic content can introduce error, particularly with regard to the LVDT null position. Figure 10 illustrates the circuit of Wein-oscillator for getting pure sinusoidal signal.

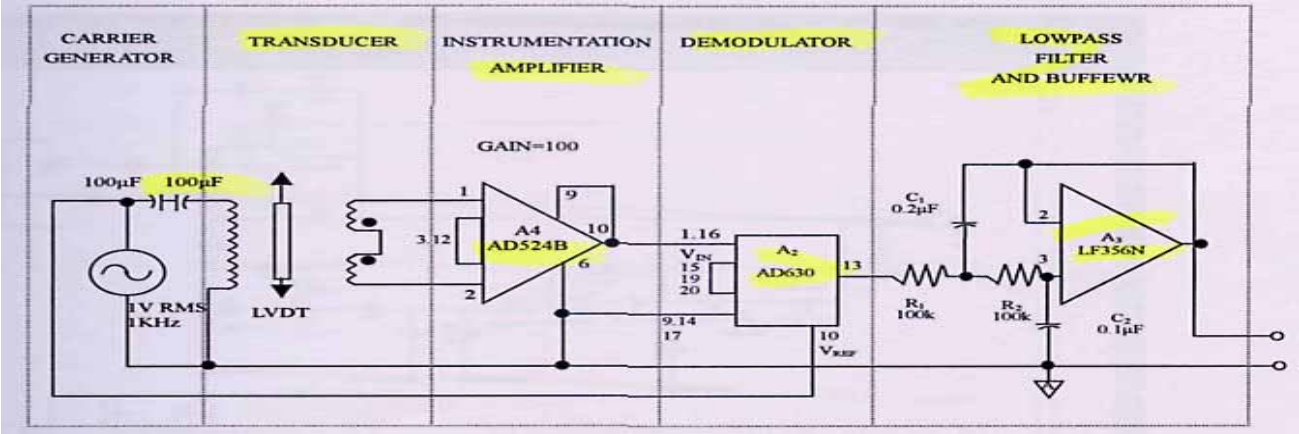


FIGURE 9
THE CIRCUIT BLOCK DIAGRAM OF LVDT AND ITS SIGNAL PROCESSING CIRCUIT.

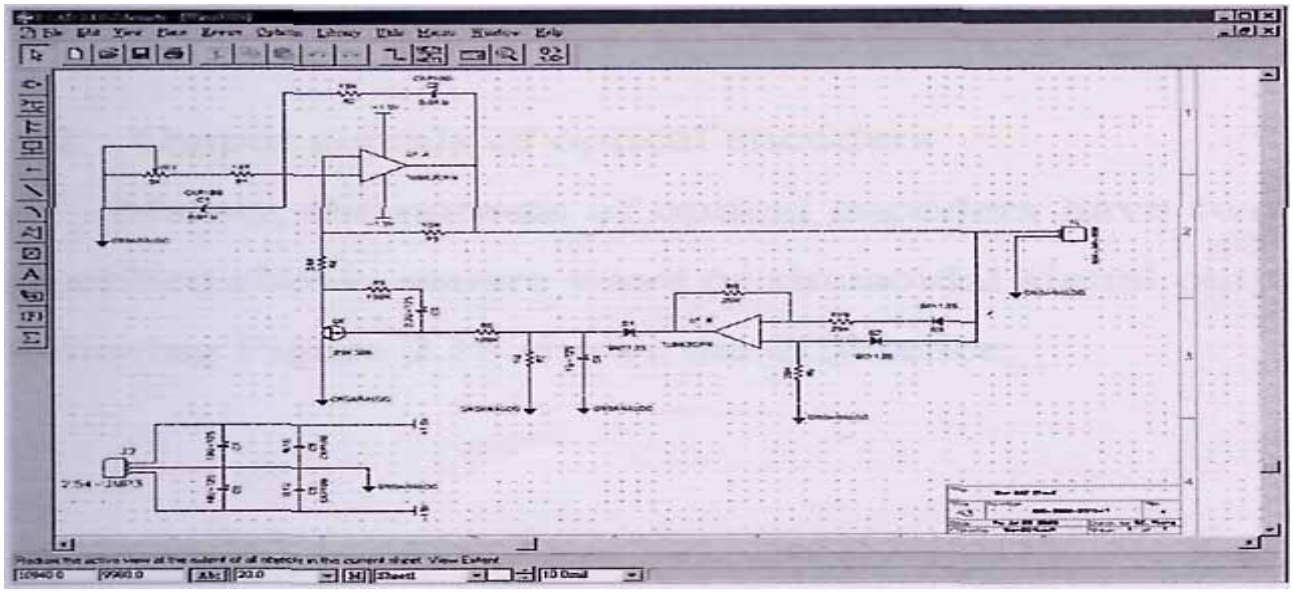


FIGURE 10
CIRCUIT DESIGN OF WEIN-OSCILLATOR.

Linear and Rotary Encoders and Output Signals: Linear encoder (or linear scale) and rotary encoder are employing the relative motion of two narrow gratings. The intensity of light will produce varied square or sinusoidal wave periodically. Varied signal of every cycle is corresponding to the various one narrow grating. To count the cycle number of intensity variation, we will know how many narrow grating have been moved. And we can get the corresponding displacement or rotary angle from the count number. For the goal of getting more accurate, the type of encoder of which has sinusoidal signal out will be better. In other words, user can use our interpolation circuit for dividing the variation more tiny. Mainly, the outputs of optical encoders have two types as described above: square wave or sinusoidal signal output. Figure 11 shows the difference. The phase difference either of Ua_1 and Ua_2 (for the type of square wave output), or signals of A and B (for the type of sinusoidal signal output) approximate 90 degrees. The latter type is quite suitable for our application. The square wave type output can not be subdivided further larger, thus it is not suitable for our design.

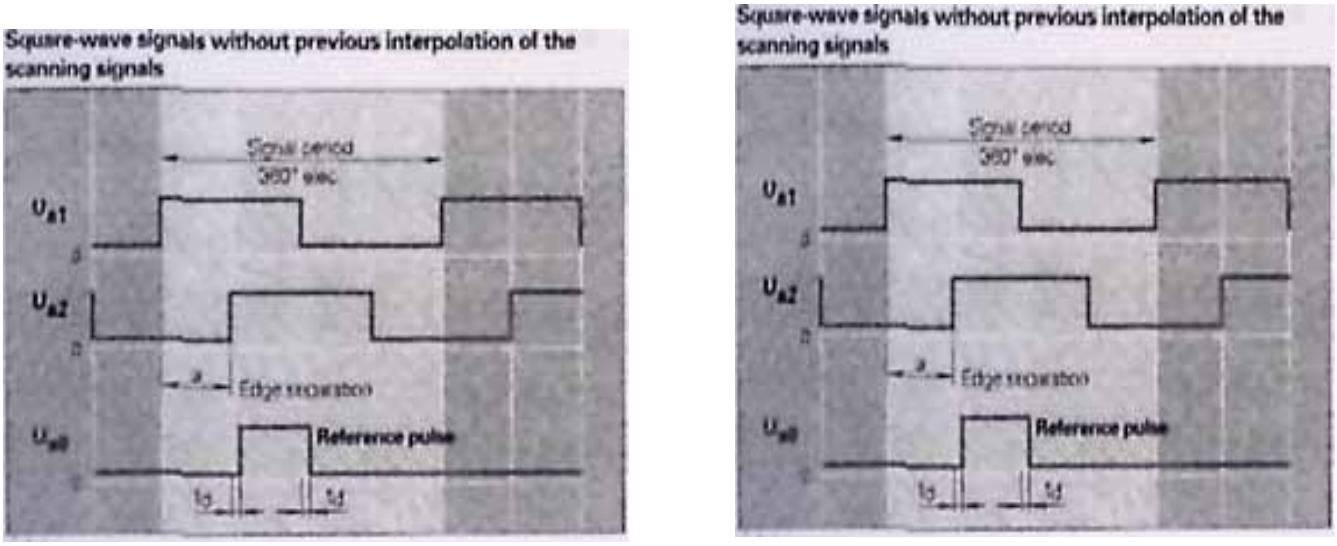


FIGURE 11
THE MAIN OUTPUT SIGNALS OF ENCODERS (FROM HEIDENHAIN CATALOG)

High Speed 8051 Microprocessor Application: For getting shorter response time, we tried to use high speed microprocessor. In the meanwhile, we are more skilled in using 8051 microprocessor for applications. By this way, we choose the DS87C520 microprocessor of which manufactured by Dallas®. The DS87C520 is a fast 8051 compatible microcontroller [12]. It features a redesigned processor core without wasted clock and memory cycles. As a result, it executes every 8051 instruction between 1.5 and 3 times faster than the original for the same crystal speed. Typical applications will see a speed improvement of 2.5 times using the same code and the same crystal. The DS87C520 offers a maximum crystal speed of 33 MHz, resulting in apparent execution speeds of 82.5 MHz (approximately 2.5X). The DS87C520 is pin compatible with all three packages of the standard 8051 and includes standard resources such as three timer/counters, serial port, and four 8-bit I/O ports. It features 16K bytes of EPROM with an extra 1K byte of data RAM. In our study, we use one DS87C520 microprocessor to generate 500 ~ 5K Hz pluses, and also receive higher frequency pulses of interpolation output by another DS87C520 board of which includes display the count result on LCD. But the input frequency range is still limited by the speed of DS87C520 even applying the crystal with the maximum frequency recommended by data sheet. By the other 8051 board, we deal with the count number obtained and display the results.

He-Ne Laser Interferometer Design: The classical method of measuring distance and little displacement is the Michelson interferometer method, which was first introduced by Albert Michelson in 1881 [13]. In 1887 a famous Michelson-Morley experiment was performed to detect the possible changes in the speed of light relative to the earth motion through space. By this experiment that Michelson got the first Nobel Prize in physics of the United States. Now, this simple and versatile instrument still plays a significant basis in length and dimensional measurements. The Michelson interferometer, shown in Figure 12, is based on division of amplitude. The optical source is incident onto a beam splitter (BS) and is then split into two beams. One goes to reference mirror and then returns to the BS again; the other transmits through a compensator to the target mirror and also returns to the BS. Both of them interfere at the BS when they are recombined. The interference signal is then received by a photo-detector. When both of the mirror images are completely parallel, the interference fringes appear circular. If these mirror images are slightly inclined to each other a strip-like fringes are formed across the field of view. As the target moving, the optical path difference is changed also. This change results in the phase shift, which is the parameter applied in length measurements. Many years till now, most interferometers use the He-Ne laser the with 633 nm wavelength as the optical source for its properties of high-stable, high-visible, and wonderful coherence length. It also provides a suitable wavelength in most applications in the range from nanometers to meters.

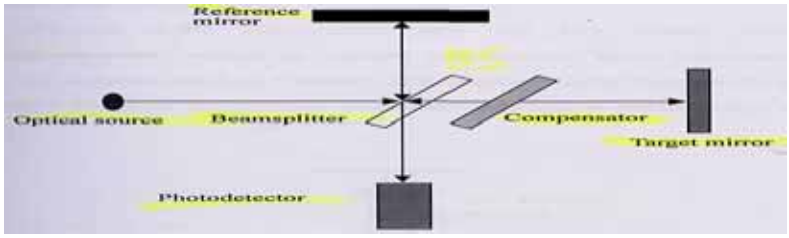


FIGURE 12
SCHEMATIC OF MICHELSON INTERFEROMETER

Fringe Counting Method: Since any additional half-wavelength optical path will produce once more interference, and then the fringe would be detected by the photo-detector in the interferometer as shown in Figure 12. Actually, the fringe is sinusoidal waveform when you inspect from the output signal of photo-detector by using current-to-voltage preamplifier. From counting the interference fringes, then one can get how much the optical path difference. The optical path of the system illustrated in Figure 12, is Michelson type interferometer with quadrature signal output. An un-stabilized He-Ne laser was used as light source. The *k / 2* retardation wave plate is placed before the reference reflector in order to obtain circularly polarized retardation. The combined radiations reflected from the reference reflector and target reflector will impinge on the polarized beam splitter PBS and then produce vertical and horizontal radiations with 90° phase difference. When the distance, i.e., optical path length from the reference reflector to the BS and then from the target reflector to the BS, is changed, the wave intensity will also change and can be detected by the photo-detectors PD1 and PD2.

Conjugate-Symmetric Quadrature Phase Interferometer: The other laser interferometer we developed quadrature phase interferometer (QPI) is shown in Figure 13. The detectors X_2 and Y_2 will detect the other wave intensity changes with a phase difference of about 180° from $X_1$and Y_1.The wave intensities of the detector X_1, Y_1, X_2, and Y_2 are given as follows, respectively.

$Vx_1 = h + a \cos(\theta)$, this equation is the same as (1)
$Vy_1 = k + b \cos(\theta - \varphi)$, this equation is the same as (2)
$Vx_2 = [h - a \cos(\theta)]/2$
$Vy_2 = (k - b \cos(\theta - \varphi)]/2$

In ideal case, we can design an electronic circuit to obtain $Vx = Vx_1 - 2Vx_2$, and $Vy = Vy_1\ 2Vy_2$, then we get
$Vx = 2a \cos(\theta)$ (3)
$Vy = 2b \cos(\theta - \varphi)$ (4)

Assuming that the gains of the four detectors are equal, the output shape of *Vx* vs. *Vy* should be a circle. This can be verified by inspecting the intensity from the oscilloscope in X-Y mode. The QPI normally can be applied in the range of 1m, and its 0.15nm accuracy can be reached [15]. We will show the experimental result of applying this interferometer to calibrate dial indicator calibrator in next chapter.

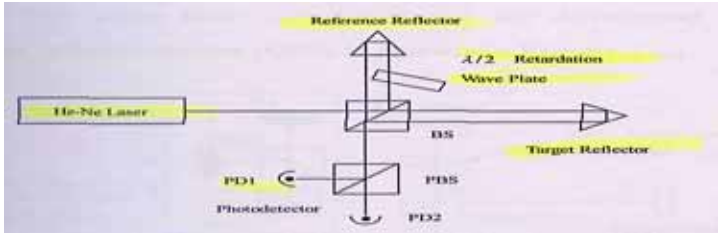


Figure 13
INTERFEROMETER USED IN LOW FREQUENCY VIBRATION CALIBRATION SYSTEM.

Mechanism Design for Laser Interferometer: The compact mechanism of the QPI, as shown in Figure 14, is designed for the applications of metrology.

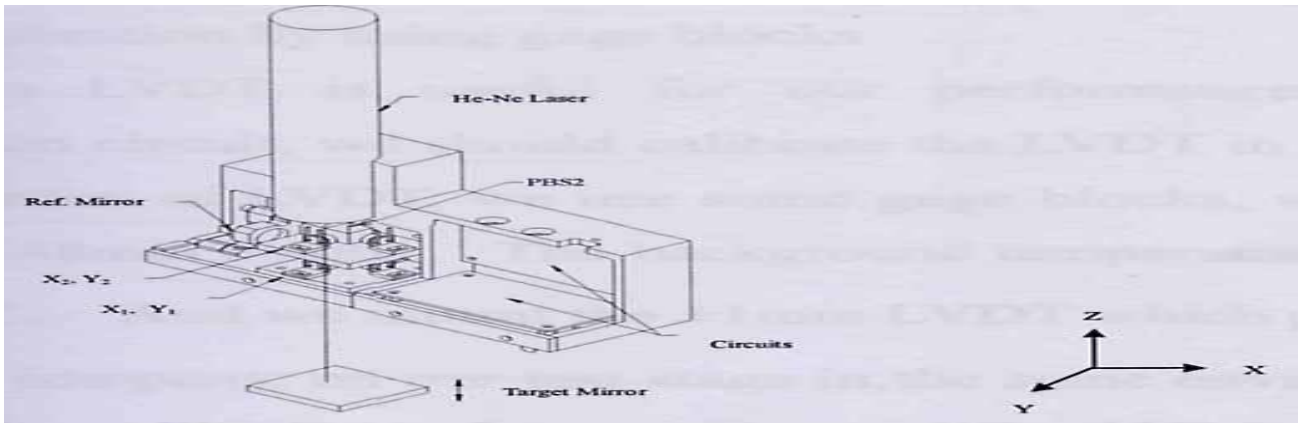


FIGURE 14
THE COMPACT MECHANISM CONSTRUCTION OF OUR QPI

EXPERIMENTAL RESULTS

In this section, we will present the measurement result including simulation and experimental setup in part 1, we will describe how to make LVDT calibration, which will be used to verify the performance of interpolation. In part 2, some results of simulations and practical experiments for interpolation circuit will be presented. In part 3, the most import tests for the interpolation circuit by using rotary encoder will be presented. Some results applying laser interferometer to calibrate dial indicator calibrator and vibration pick-up will show in part 4. And in the last part, we will present the verification result of performance test for interpolation circuit by using linear encoder.

LVDT Calibration by Using Gage Blocks: Due to LVDT is useful for our performance test of interpolation circuit, we should calibrate the LVDT in advance. For calibration of LVDT, we use some gage blocks, which are 1.005 to 1.48mm height. The background temperature drift is about ± 1℃. And we mount the ± 1 mm LVDT which produced by RDP® company, on our test stage in the same environment. We start the calibration after our warmed the LVDT up more than 30 minutes. Figure 15 shows our setup for the LVDT calibration by using gage blocks. We used 8 gage blocks of which 1.005, 1.05, 1.15, 1.19, 1.25, 1.35, 1.45, and 1.48mm for this calibration, individually. Figure 16 presents the scale factor calibration result of the LVDT.

FIGURE 15
SETUP FOR THE LVDT CALIBRATION BY USING GAGE BLOCKS

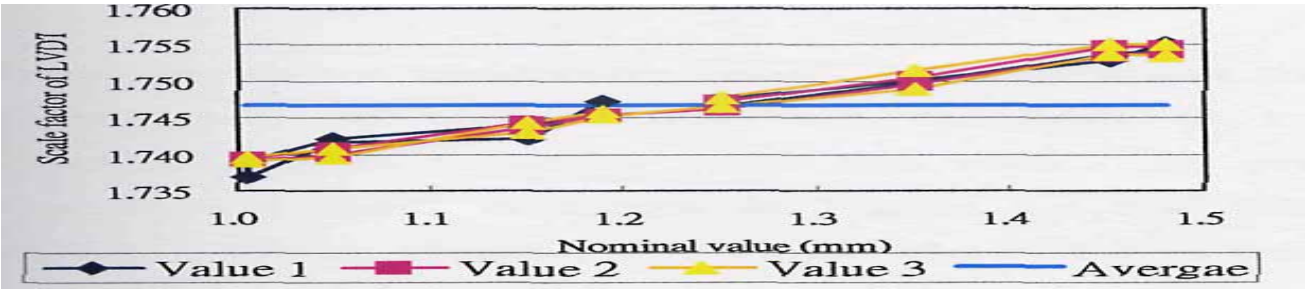


FIGURE 16
CALIBRATION RESULT OF LVDT SCALE FACTOR

Interpolation Circuit: This section teaches the student how to test the performance of interpolation functions by the way of simulations and practical experiments. The digital noise filter is the input stage of our interpolation circuit. Simulation result for this stage is shown in Figure 17, where OSC-10 MHz, DPA, and DO, are the clock, input signal, and output signal, respectively. We can forecast the noise can be reduced or not. From the above simulation result, we can know that the input frequency of signal DPA will be limit to half of OSC 10 MHZ. This result is what we wish. In practical experiment, our result is shown in Figures 18 and 19, where channel 1 is clock, channel 2 is the input signal, and channel 3 is the output signal. We reach our goal.

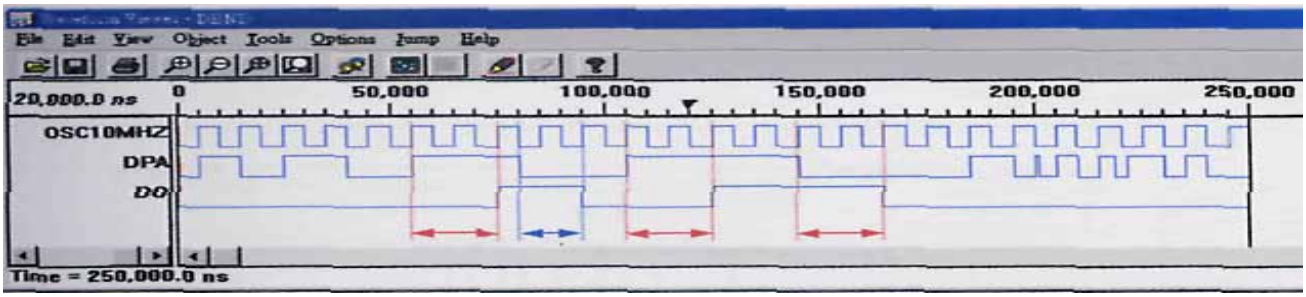


FIGURE 17
SIMULATION RESULT OF THE DIGITAL NOISE FILTER

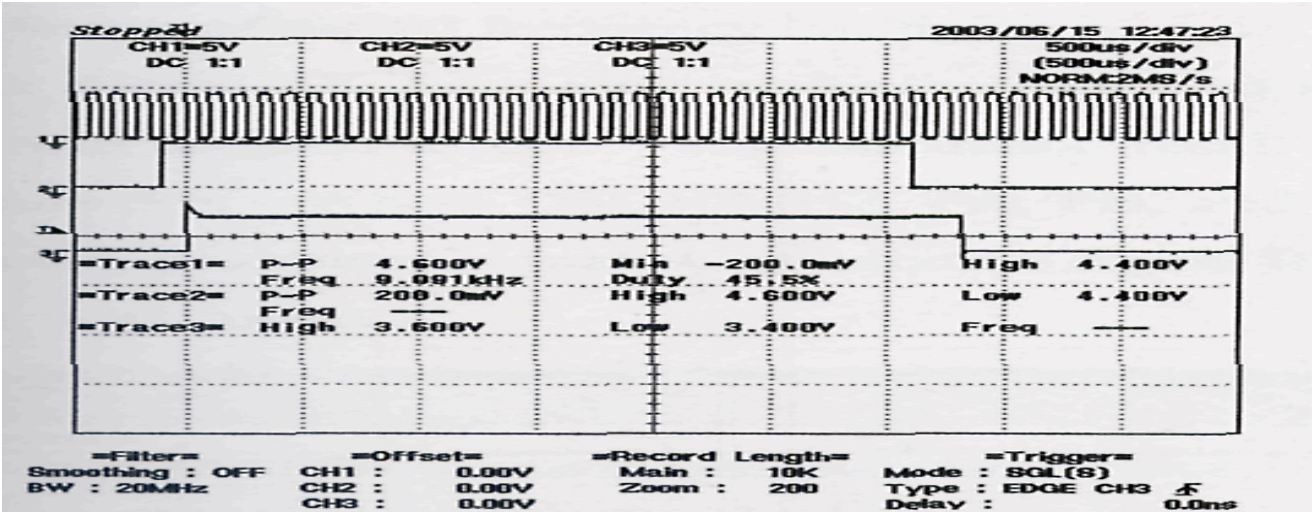


FIGURE 18
THE RESULTS WHEN THE FREQUENCY OF CLOCK IS 9.09 KHZ, AND DPA 186 HZ

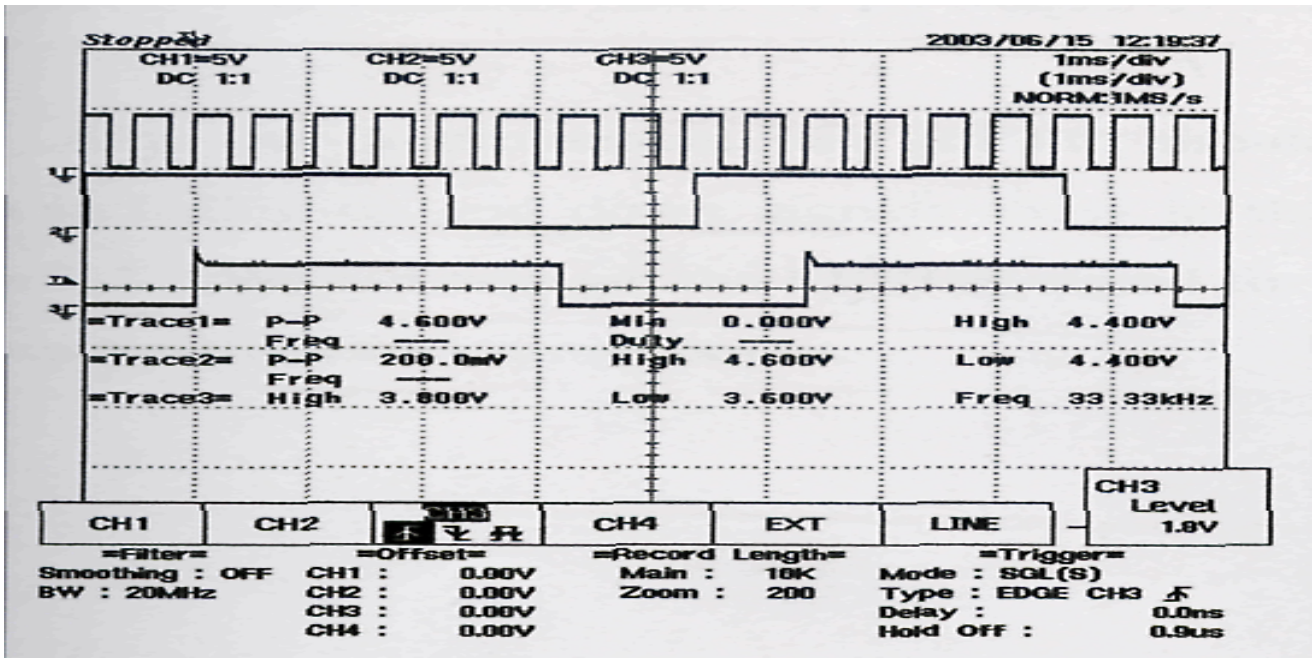


FIGURE 19
THE RESULTS WHEN THE FREQUENCY OF CLOCK IS 1865 HZ, AND DPA 932 HZ.

Results of Interpolation Circuit: The simulation results of interpolation circuit are as shown in Figures 20-23. The whole prototype interpolation circuit is shown in Figure 24 where the main interpolation circuit is in the upper part. Some of the results of practical experiment are presented as shown in Figures 25-28.

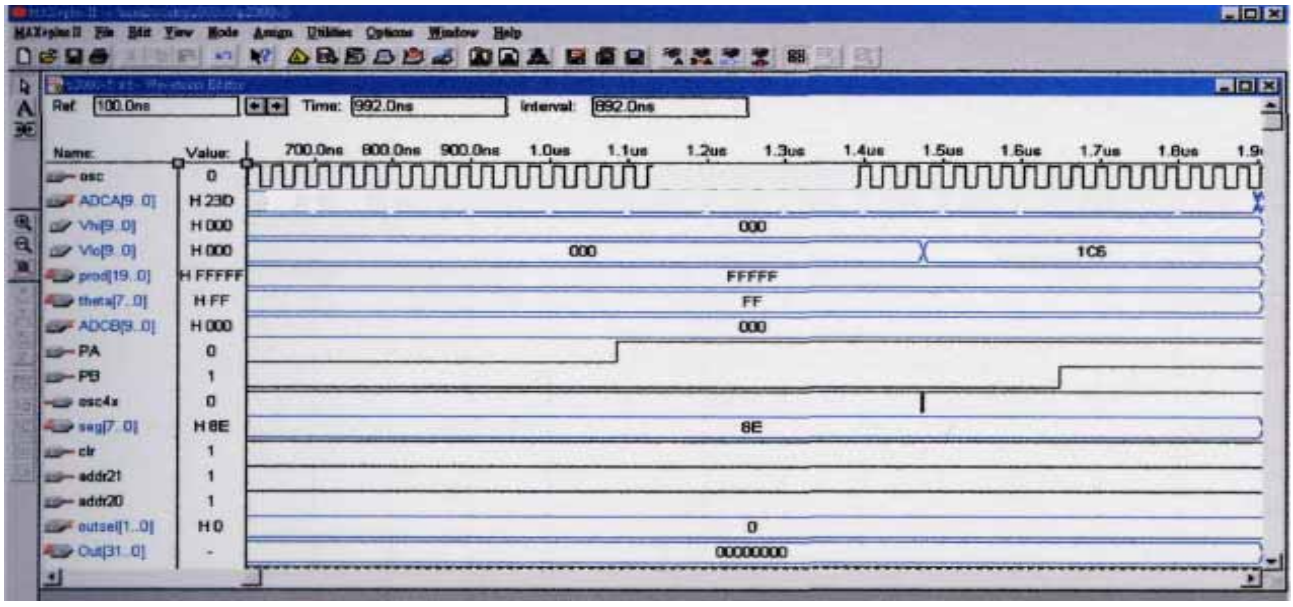


FIGURE 20
SIMULATION RESULT WITH REFERENCE INPUT VHI BE "LOW"

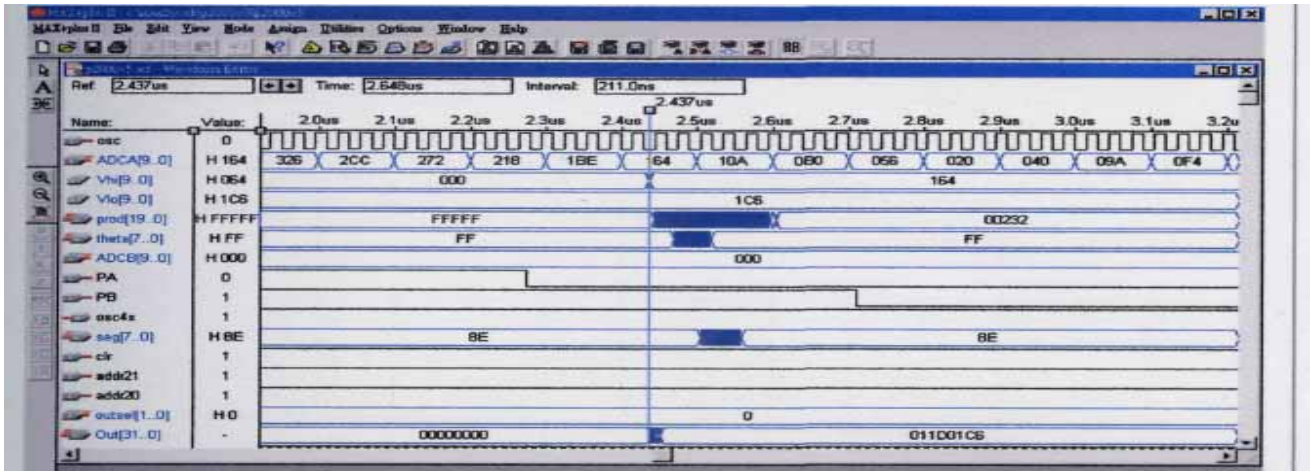


FIGURE 21
SIMULATION RESULT WITH REFERENCE INPUT VHI CHANGED TO "HIGH"

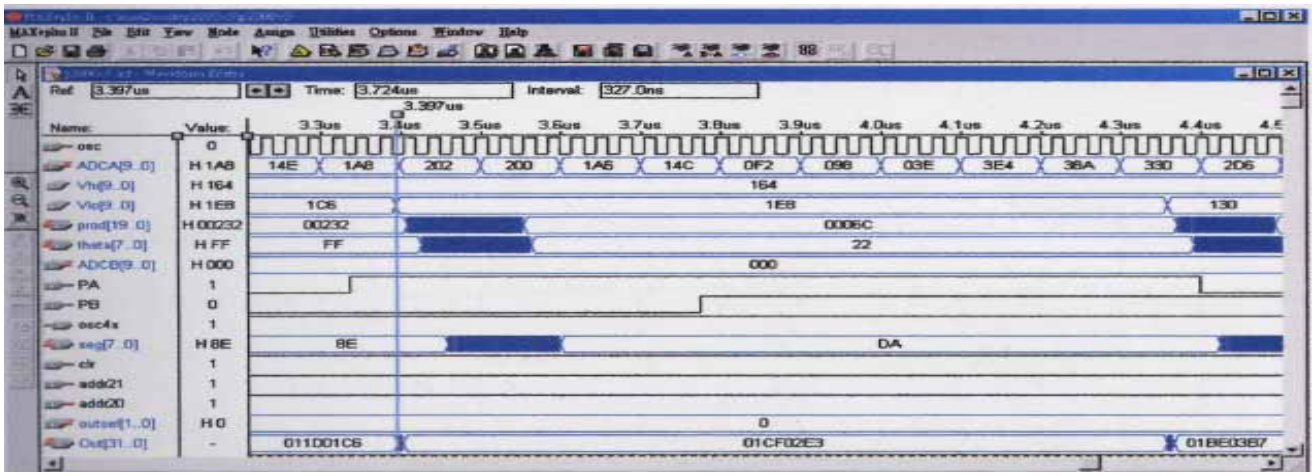


FIGURE 22
SIMULATION RESULT OF SIGNAL VARYING.

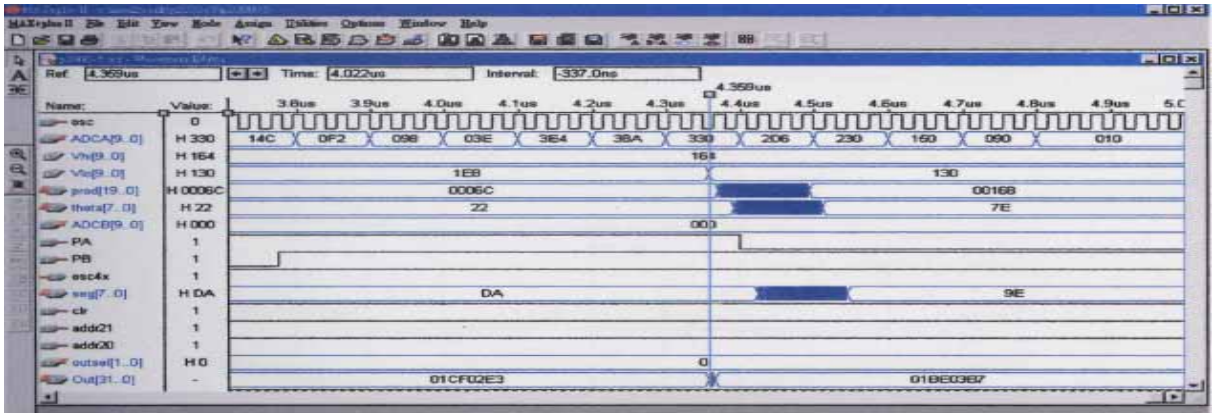


FIGURE 23
SIMULATION RESULT OF SIGNAL CHANGING OVER AND OVER AGAIN

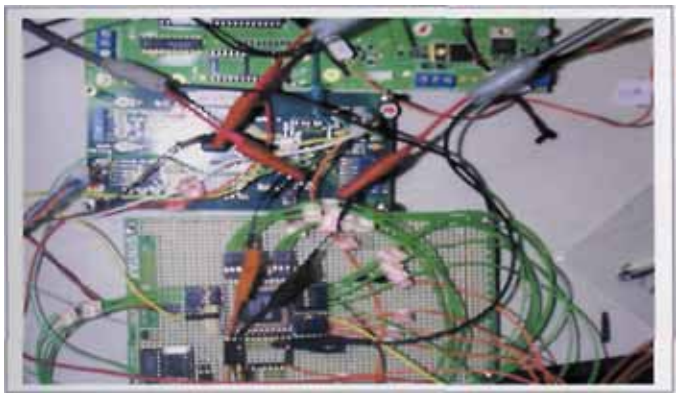


FIGURE 24
MAIN INTERPOLATION CIRCUIT AND 4X FREQUENCY MULTIPLIER AND UP / DOWN COUNTER

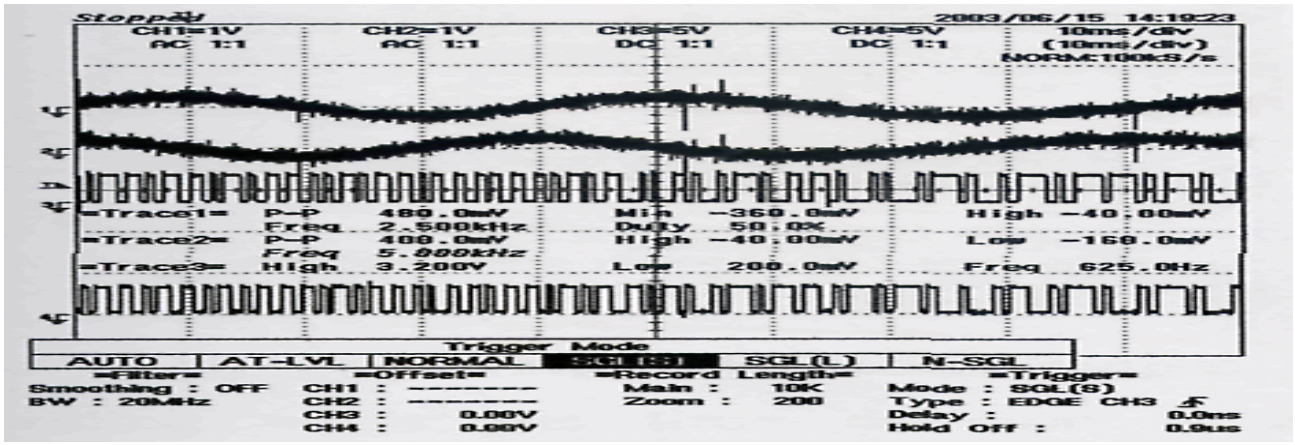


FIGURE 25
RESULT OF PULSE OUTPUT IN 25-TIMES SUBDIVIDING

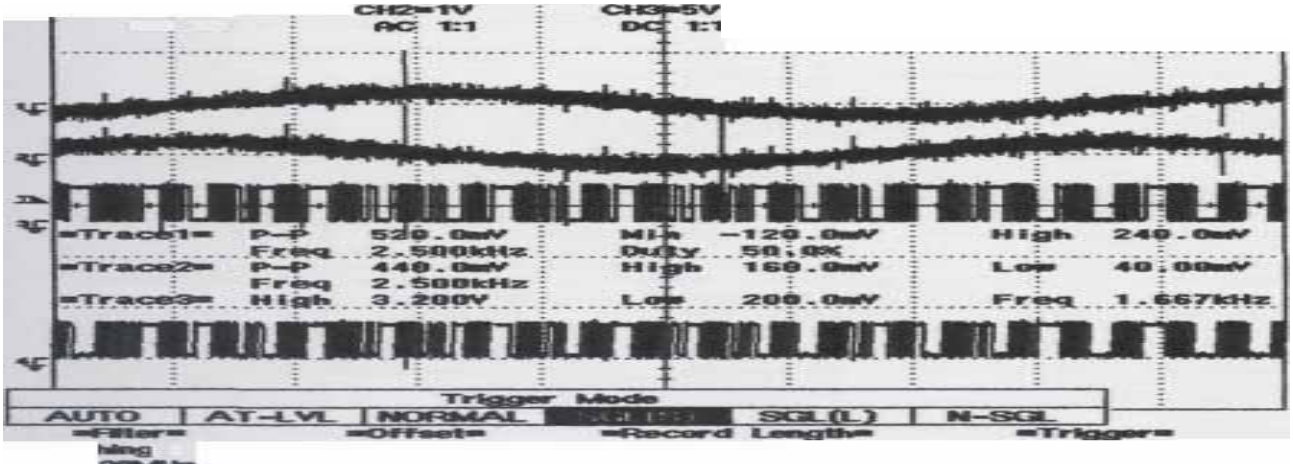


FIGURE 26
RESULT OF PULSE OUTPUT IN 100-TIMES SUBDIVIDING

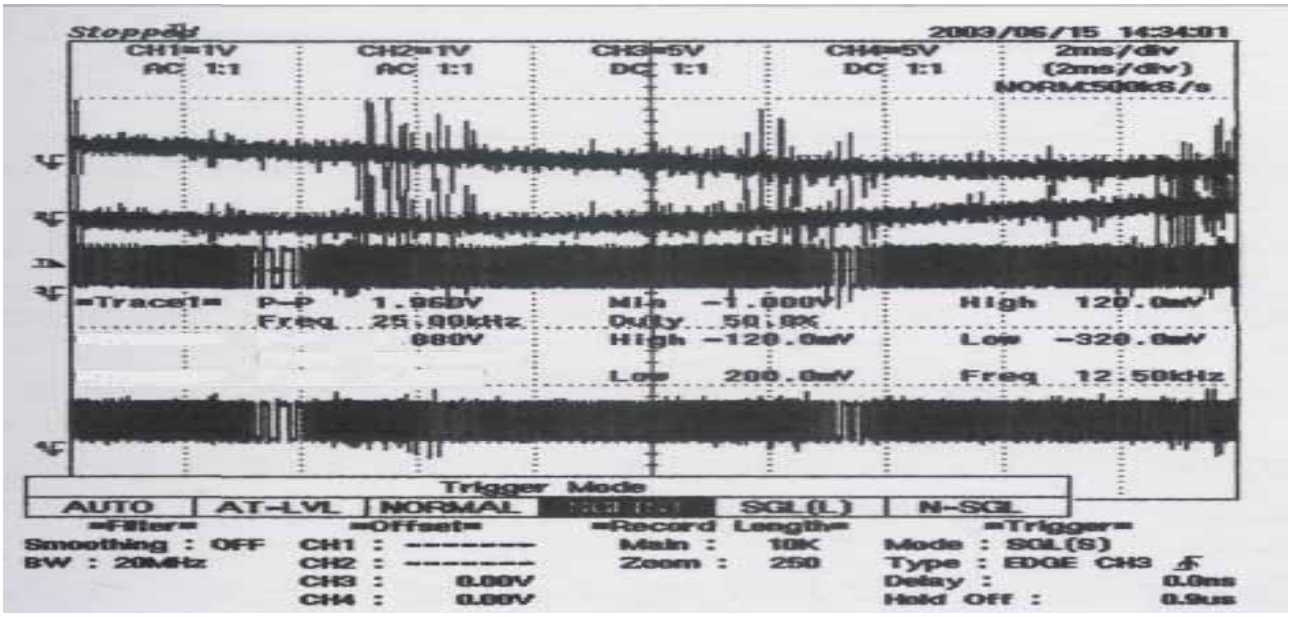


FIGURE 27

RESULT OF PULSE OUTPUT IN 400-TIMES SUBDIVIDING WHILE THE TIME DIVISION IS 2MS/DIV SET IN OSCILLOSCOPE

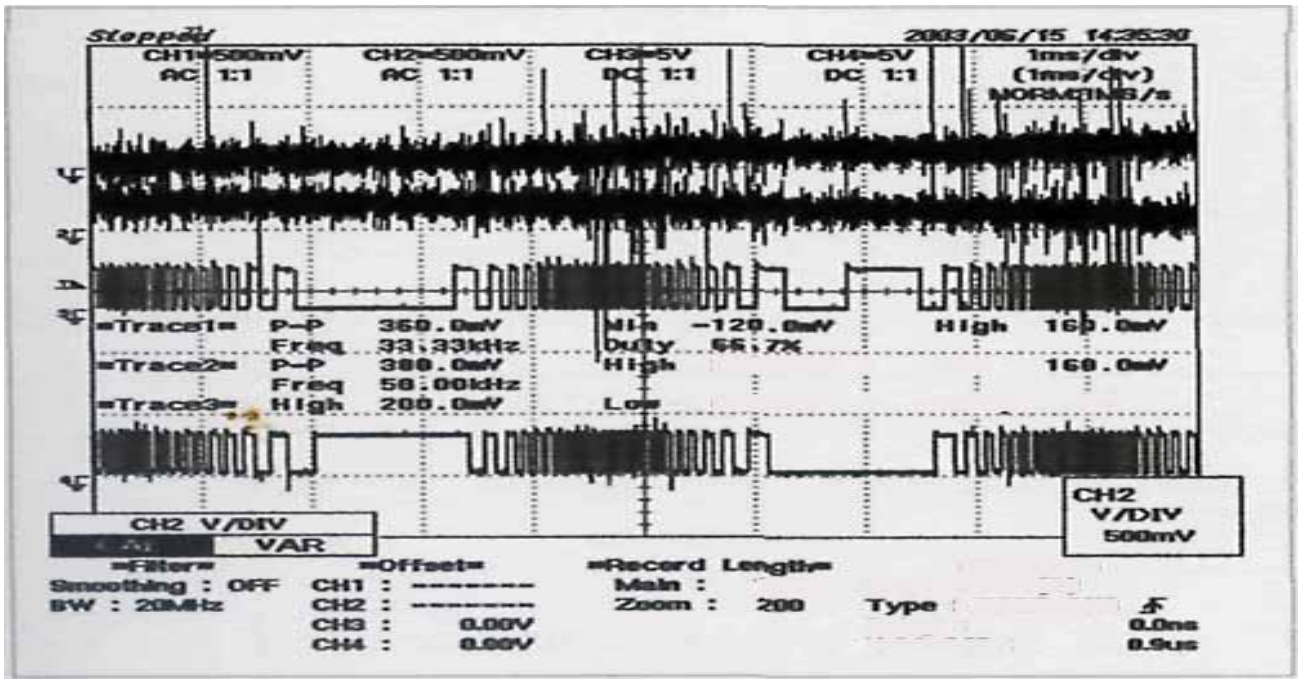


FIGURE 28

RESULT OF PULSE OUTPUT IN 400-TIMES SUBDIVIDING WHILE THE TIME DIVISION IS 1 MS/DIV SET IN OSCILLOSCOPE

Test Results of Rotary Encoder: This section briefs how to check the performance of interpolation by using the rotary encoder and the mechanism described before. We tried to send pulses in different frequency, and different pulse number. In addition, we also switch the times of interpolation.

Comparison in Same Turn but Different Subdivision: When we send the same pulses to drive the stepping motor in the test mechanism, the number of turns should be the same, theoretically. Figure 28 shows the test results while same turn, but different frequency and subdivision. The maximum value is 0.332%, and minimum value is 0.031%. The percentage is equal to the standard deviation divided by count of average with 11-times measurement. On the other hand, our changing the pulse number and times of interpolation will lead to different count number we will get, proportionally. The test result is shown in Figure 29 by subdividing - percent chart in the same 1 KHz pulse. The maximum value is 1.245%, and minimum value is 0.013% in the result.

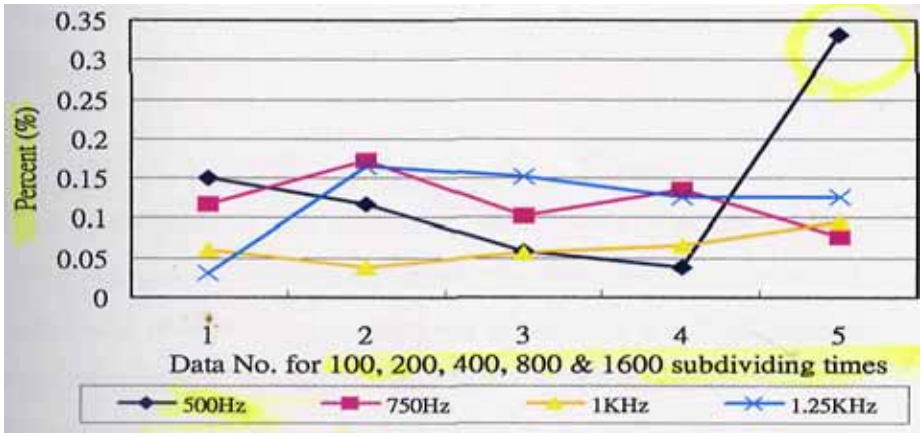


FIGURE 29
TEST RESULTS WITHIN THE SAME TURN, BUT DIFFERENT FREQUENCY AND SUBDIVISION.

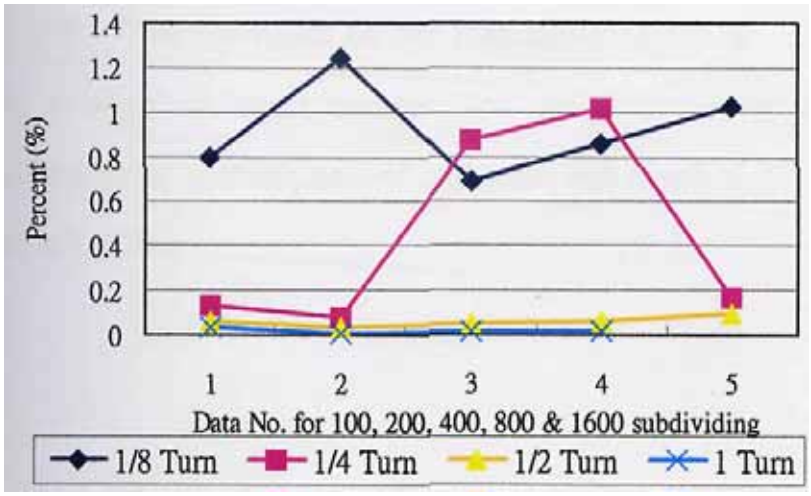


FIGURE 30
TEST RESULTS WITHIN THE SAME TURN, WITH THE SAME FREQUENCY AND SUBDIVISION.

Comparison in Same Speed but Different Turn: This section briefs the result by using the same 500 Hz pulse driving but different pulse number to drive the stepping motor with the test mechanism mentioned. The test results are shown in Figure 31-32. In the former case we get the average of count number and deviation with the subdividing times 1600, half of one turn, and the nominal count number is 819200**.** While in the latter one we get the average of count number and deviation with the subdividing times 100, half of one turn, and the nominal count number is 51200. From the above results of count number, we can find that the results of count number are quite like the sharp of a saw. And we found the situation is mainly resulting from the alignment of shaft coupling. We measured the displacement of surface on the rotary encoder, and found a ± 102 um displacement by using dial indicator with 1um resolution. The experimental setup is as shown in Figure 3.3.

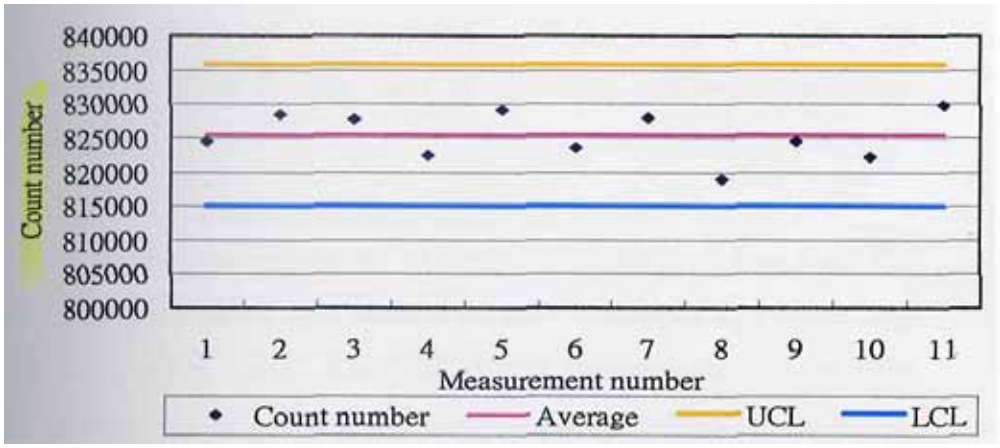


FIGURE 31
THE TEST RESULT FOR 11- TIMES MEASUREMENT WITH SUBDIVIDING TIMES 1600, AND HALF OF ONE TURN.

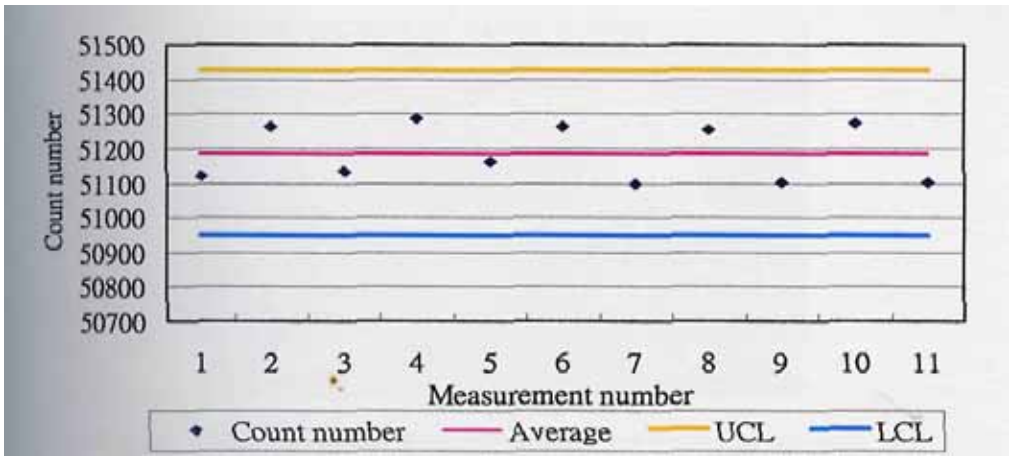


FIGURE 32
THE TEST RESULT FOR 11- TIMES MEASUREMENT WITH SUBDIVIDING TIMES 100, AND HALF OF ONE TURN

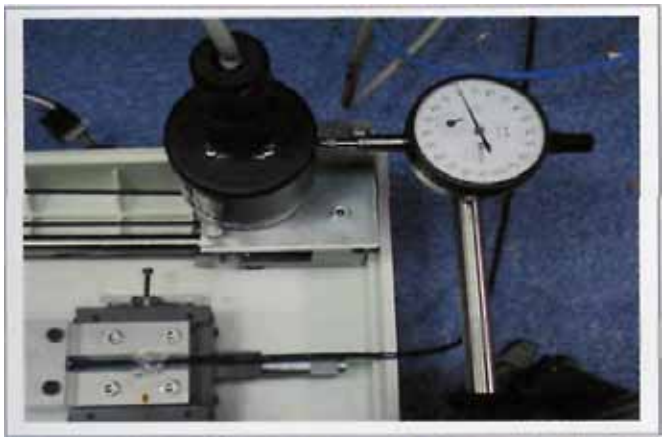


FIGURE 33
INSPECTING THE ALIGNMENT BY USING DIAL INDICATOR.

Conjugate-Symmetric He-Ne Laser Interferometer: This section teaches the students how to establish the calibration system for dial indicator calibrator. After the QPI is developed, we have to take a performance test by using dial indicator calibrator as well as data acquisition system. Our setup for the test is as shown in Figure 34. The performance of QPI can be represented by its repeatability. We take four times of repeated measurements and calculate the deviation as the repeatability of QPI. On the other hand, the resolution of QPI can be promoted to A /4096 by replacing the target mirror with a retro-reflector. Figure 35shows four sets of measurement in the range of 5 mm. And Figure 35 shows the deviations of the measurements. The background vibration , temperature drift , and relative humidity are about -91.53 dBG to -81.02 dBG , ± 0.2°C ,and ± 2.5% , respectively , during the QPI performance test. Usually, the calibration of dial indicator can be finished within two hours, but we took repeated measurements in seven hours to obtain the long term stability of QPI. The result is shown in Figure 36, where the maximum and minimum values are about 32nm and -17 nm, respectively.

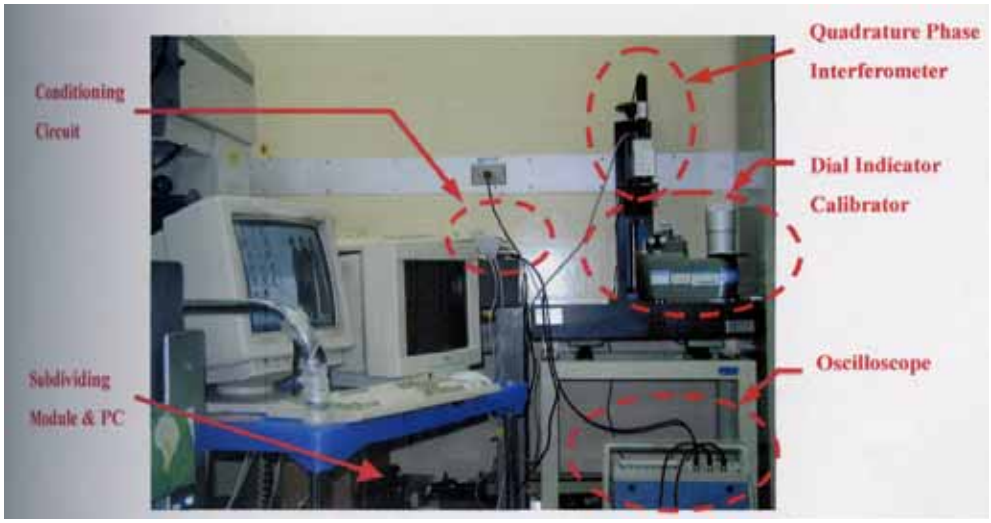


FIGURE 34
SETUP FOR CALIBRATION THE DIAL INDICATOR CALIBRATOR BY USING QPI ARMED WITH SUBDIVIDING MODULE

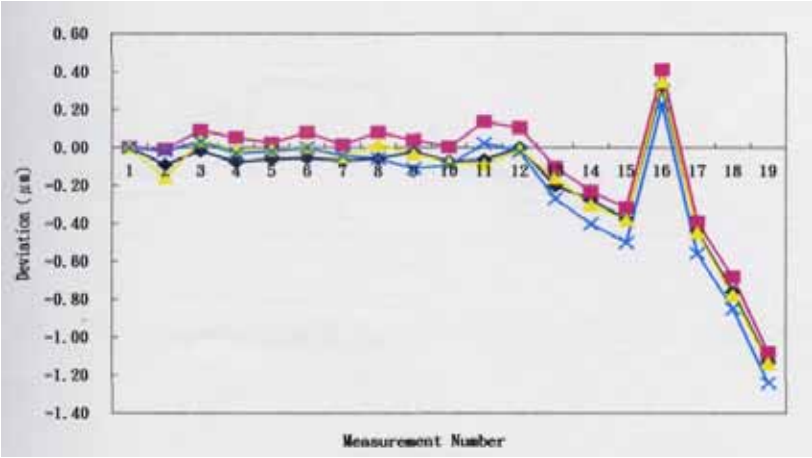


FIGURE 35
RESULT OF TEST FOR THE NOMINAL VALUE AND DEVIATION WITH FOUR SETS OF MEASUREMENT IN THE RANGE OF 5 MM.

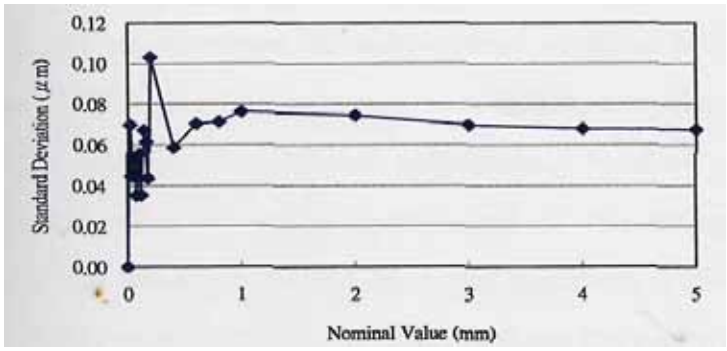


FIGURE 36
THE STANDARD DEVIATIONS OF THE MEASUREMENT

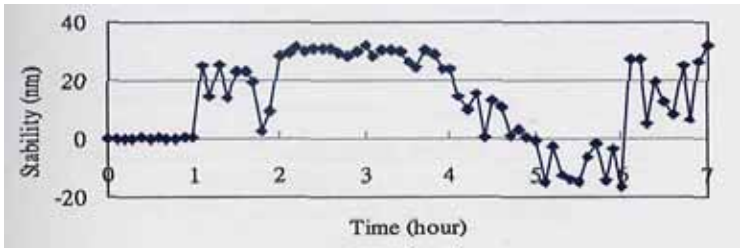


FIGURE 37 THE
MEASUREMENT RESULT OF THE LONG TERM STABILITY OF QPI

Measuring System Verification: For verity the performance of subdividing module, we also calibrated the LVDT by using the test mechanism, encoder, dial indicator, 8051 catching board, and subdividing module. We used the dial indicator, which is needle-type as the reference. And we drive the stepping motor in pulse numbers 12500, a quarter turn, 750 Hz and 1250 Hz. And we defined the calibration factor of LVDT as

$$Calibration\ factor = \left(\frac{\Delta Variance\ of\ LVDT}{\Delta Variance\ of\ Count\ number} \right) \times 100000$$

We take six times repeated measurements and calculate the calibration factor. The result is as shown in Figure 38, where the maximum value is 1.04486, and the minimum value is 1.03866.

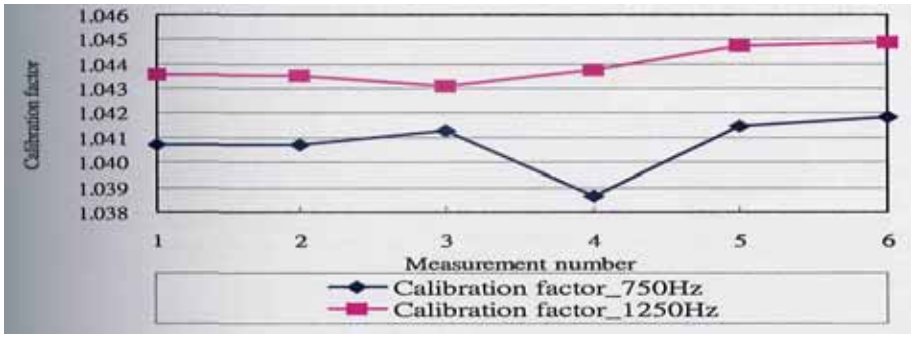


FIGURE 38
REPEATABILITY TEST RESULT OF LVDT CALIBRATION FACTOR

DISCUSSIONS

Deviation of Measuring System: From the experiment results, we can get the deviation when we test the subdividing module by using test mechanism and rotary encoder. The numerical results are as shown in Tables1 and 2, which present different test conditions. The results are corresponding to Figures 29and 30.

Data No.	500 Hz	750 Hz	1 KHz	1.25 KHz
1	0.15082661	0.11742089	0.06015199	0.03093256
2	0.11761664	0.17137734	0.03774815	0.1657873
3	0.05788331	0.10212272	0.05680505	0.15148943
4	0.03904855	0.13561634	0.06559612	0.12620357
5	0.33232307	0.07671483	0.09611304	0.12620357

TABLE 1
STANDARD DEVIATIONS IN SAME TURN BUT DIFFERENT SUBDIVIDING TIMES

Data No.	1/8 Turn	1/4 Turn	1/2 Turn	1 Turn
1	0.794562	0.12924	0.060152	0.031812
2	1.244762	0.079231	0.037748	0.012902
3	0.68758	0.878622	0.056805	0.013808
4	0.853616	1.018655	0.065596	0.013609
5	1.027556	0.162204	0.096113	

TABLE 2
STANDARD DEVIATIONS IN SAME PULSE FREQUENCY BUT DIFFERENT SUBDIVIDING TIMES

Improvement for Measuring System: For improving our LVDT measuring system and QPI, we have to reduce the influences coming from some error sources. For reduce the error from subdividing module, we should minimize the electronic noise, and increase the amplitude of input signals. For reduce the error from the positioning, we can change open-loop control to close-loop control, or change stepping motor to servo motor. The situations of missing step and stall should be avoided. Figure 39 shows the counting error from the situation of missing step, where Channel 1 is the encoder output signal, channel 2 and channel 3 are the quadrature signal output from subdividing module. We also have to take care of the environment vibration especially in setting higher subdividing times. Figure 40 shows the influence coming from vibration that we should care about, where Channel 1 shows the encoder output signal, channel 2 and channel 3 show the quadrature signal output from subdividing module.

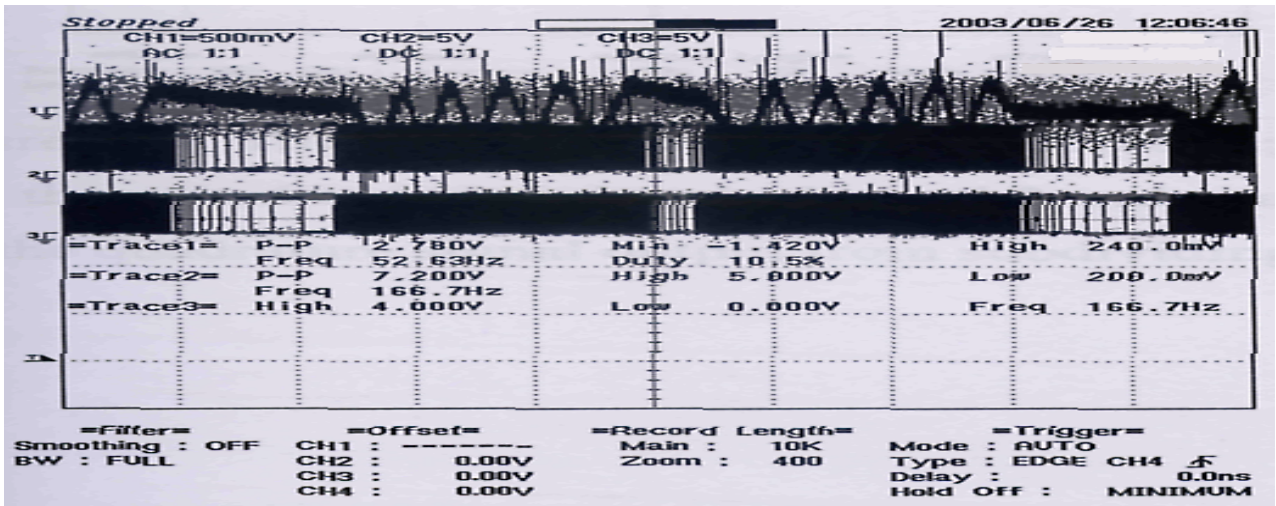


FIGURE 39
THE COUNTING ERROR COMES FROM THE SITUATION OF MISSING STEP

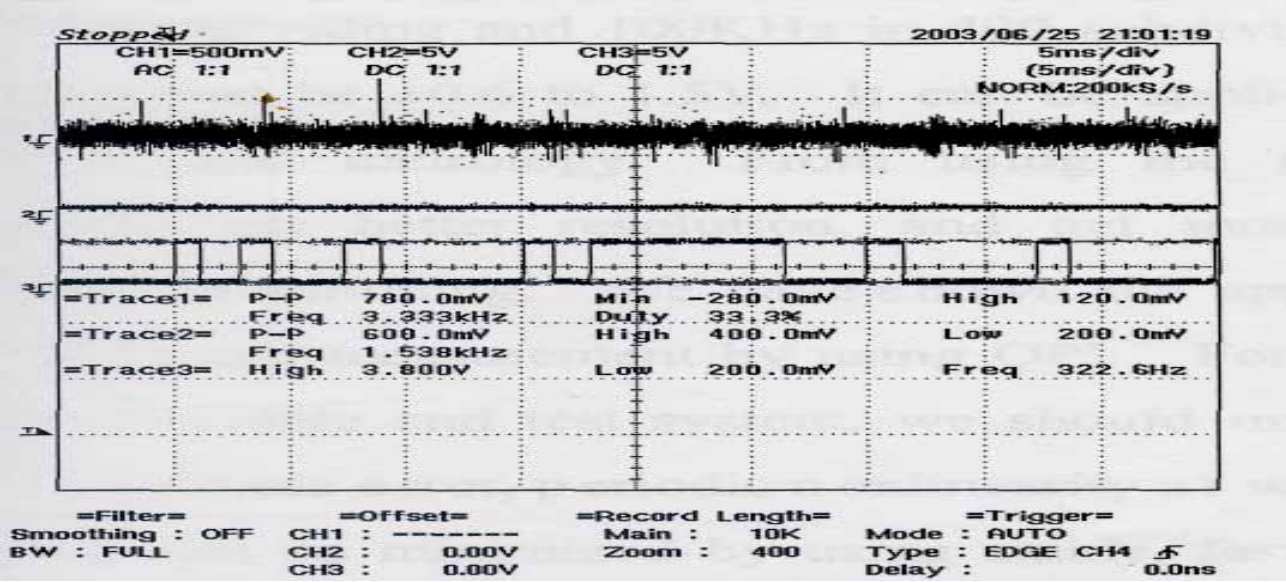


FIGURE 40
THE RESULTS OF INFLUENCE COMING FROM VIBRATION

CONCLUSIONS

In this precision measurement equipment improvement teaching program for the senior students, we have achieved success in 100 to 1600 subdividing. And the input frequency of quadrture signal can up to 5 KHz in 1600 subdividing and 100 KHz in 400 subdividing. The amplitude range can be ± 0.6 to 1.5V. It can be applied in some industrial fields and metrology. From using the subdividing module, we can get better resolution, and get more accurate measurement and positioning. We have shown the application in calibrating LVDT and measurement by using QPI. For improving the subdividing module and test system, we should minimize the signal noise, electronic error, periodic nonlinearity as well as can. Electronic error can be minimized by using stable, fast and noise reduced circuits. Nonlinearity can be minimized by having better alignment, better laser source, and ultra low leakage polarized beam splitter. And fine tilting adjustment can minimize the leftover ghost-reflections.

ACKNOWLEDGEMENT

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