A MOSFET Design Laboratory

Authors:

Ahmet Bindal, Computer Eng. Dept., San Jose State University, San Jose, CA 95192, ahmet.bindal@sjsu.edu
David Parent, Electrical Eng. Dept., San Jose State University, San Jose, CA 95192, dparent@email.sjsu.edu
Lili He, Electrical Eng. Dept., San Jose State University, San Jose, CA 95192, lhe@email.sjsu.edu
Salih Kilic, Electrical Eng. Dept., San Jose State University, San Jose, CA 95192, salihkilic@gmail.com

Abstract *— The authors have developed a MOSFET design laboratory to enhance a graduate level Device Physics course at San Jose State University using Silvaco's device design tools and simulation platform. The laboratory experiments guide students through designing enhancement type NMOS and PMOS transistors. Prior to the design, a technology consisting of the power supply voltage, oxide thickness, gate material and minimum channel length is defined. Using Silvaco's ATLAS Device Design Environment, the design methodology starts with designing 1.0 μm effective channel length NMOS and PMOS transistors with specified threshold voltages. In the next step, the threshold voltage (V_T) drop-off is investigated as the effective channel length is decreased towards a minimum value of 0.1 μm. A Lightly Doped Drain (LDD) design technique is demonstrated to reduce high electric fields at the drain and the resultant rate of impact ionization. The subsequent tasks analyze each transistor's body-effect and source/drain (S/D) junction capacitance. Finally, the NMOS and PMOS transistors are redesigned to decrease the V_T roll-off, body effect and S/D junction capacitance.*

Index Terms *— MOSFET Design, NMOS and PMOS Design, Transistor Design, Silvaco ATLAS Device Design and Simulation Environment.*

INTRODUCTION

Solid State Electronics is one of the most difficult subjects to teach to Electrical Engineering students, as it requires subjects ranging from elementary quantum mechanics to advanced theory of semiconductors and solids. Students taking advanced device electronics courses such as the Theory of Semiconductor Devices, often struggle with deriving lengthy equations and comprehending their meaning. Technology now demands that transistors approach quantum scale [1, 2]; therefore, academia must keep pace with this fast-evolving industry and find effective methods to teach the MOS Device Electronics.

To achieve this goal, two important issues have to be resolved. First, students must be encouraged to use commercial CAD tools for laboratory design projects. This laboratory uses Silvaco's ATLAS simulator for "real-life" transistor design projects. The ATLAS simulation environment utilizes the limited laboratory time efficiently and provides an effective method of associating analytical device equations with the actual device behavior.

The second issue is teaching students to effectively research and find information in the library instead of using the instructor's notes or the textbook. By assigning open-ended, "real-world" transistor design problems in the laboratory, students are forced to go to the library and read current technical articles to resolve various device design issues.

The device design experiments in this course differ from an earlier device design course reported in the literature [3]. To correlate the experimental data with the theoretical material, the earlier course spent too much time fabricating the device in a clean room and then measuring the device characteristics on a curve tracer. Device design courses should emphasize device physics and methods of design, not intensive device fabrication. Silvaco's device simulation tool is able to create an environment where realistic device characteristics can be measured in matter of hours if needed for comparison with various MOS transistor structures.

LABORATORY OBJECTIVES

The overall objective of this course is to link the MOS transistor theory to the actual design process in such a way that students are able to observe the transistor behavior by changing device parameters and making design trade-offs during laboratory sessions. Each laboratory exercise systematically targets optimization of the transistor characteristics one at a time and to build up the final design within specifications.

At the end of this course, four objectives will be accomplished:

Understanding the Fundamentals to Design A Conventional MOS Transistor:

- Understanding the elements that change the threshold voltage, V_T, of a MOS transistor: gate material, channel doping concentration and oxide thickness.
- Understanding the charge-sharing issue in the channel and its effect on V_T as a function of Effective Channel Length, L_{EFF}.
- Understanding the implication of body effect on V_T.
- Understanding the concept of Lightly Drain Doped (LDD) region and its effect on reducing impact ionization, gate and substrate currents.
- Understanding the effect of V_T on maximum dc transconductance, gm_{SAT}.
- Understanding the elements to reduce standby power in a transistor: the OFF Current, I_{OFF}.
- Understanding the implications of sub-threshold current on transistor's switching characteristics.
- Understanding the effect of S/D junction capacitance, C_J, on digital circuit performance.

Defining the Technology and Designing A Conventional MOS Transistor:

- Defining the technology and design specifications.
- Designing a short channel transistor that meets the device specifications for a given technology.
- Obtaining device characteristics at various channel lengths.

Enhancing the Transistor Performance:

- Reconfiguring the transistor structure to reduce charge-sharing effect and C_J for short channel transistors.
- Developing device-processing techniques to reduce body effect.

Promoting Life-Long Learning Skills:

- Encouraging students to conduct library research on new MOS transistor designs as a life-long learning skill.

LABORATORY OVERVIEW

The laboratory experiments are organized in two consecutive stages. The first stage summarizes the experiments for designing a conventional MOS transistor. The second and more advanced stage reconfigures the transistor structure in order to improve its device characteristics.

Experiment 1: Learning Silvaco's Device Design Environment and Revisiting the MOS Transistor Equations

The first experiment mainly allows students to become familiar with ATLAS, Silvaco's device design environment. The first part of this experiment has no design involvement; students are guided through sample design files in ATLAS to get familiar with this design environment. They learn how to create template files that define the transistor structure, materials involved in the structure and how to apply bias to the electrodes of the transistor for obtaining input and output I-V characteristics. One such transistor structure is shown in Figure 1.

The second part of this experiment is solely an exercise to get acquainted with the classical MOSFET equations to understand the device behavior during simulation and make design trade-offs. These equations are well known and summarized below [4]:

In linear region:

$$I_D \approx \frac{\mu C_{OX} W}{L_{EFF}}(V_{GS} - V_T)V_{DS} \qquad (1)$$

In saturation region:

$$I_D \approx \frac{\mu C_{OX} W}{2L_{EFF}}(V_{GS} - V_T)^2 \qquad (2)$$

where, threshold voltage, V_T:

$$V_T = V_{FB} + \Psi_S + \frac{Q_C}{C_{OX}}\gamma \qquad (3)$$

and oxide capacitance, C_{OX}:

$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}} \qquad (4)$$

The most important device parameters above are the ones that constitute V_T in (3): Q_C is the total ionized dopant charge in the channel, and γ is the "charge sharing ratio" or the portion of the ionized dopant not shared by the drain and source contacts. A very detailed explanation of the charge-sharing ratio can be found elsewhere [5]. Ψ_S , the semiconductor band bending voltage at strong inversion, and V_{FB}, the flat band voltage, are not as strong parameters to change the value of V_T once the technology is defined. Therefore, the channel doping concentration practically defines the value of V_T, and γ contributes only when L_{EFF} becomes increasingly small.

Experiment 2: Defining the Technology and Designing Conventional MOS Transistors

This assignment has five tasks. The first task is to define the technology to be used in designing conventional NMOS and PMOS transistors. This task also includes specifying a set of constraints for the device characteristics. Due to the space requirements of this manuscript, we will only explain the method of designing an enhancement-type NMOS transistor; we will also omit issues such as sub-threshold characteristics [6], gate-drain and gate-source capacitances [7], the ionic oxide charges and interface states [8], the OFF current, I_{OFF}, [9] and narrow width effects [10] from the design constraints.

- Power supply voltage (V_{DD}) = 1.5 V.
- Gate oxide thickness = 5 nm.
- Gate material = polysilicon.
- Gate thickness = 150 nm.
- Gate doping density = 10^{20} cm^{-3}.
- Minimum L_{EFF} = 100 nm.
- S/D regions have a peak doping density is 10^{20} cm^{-3}. The approximate junction depth should be approximately 100 nm.

The device characteristics should meet the following constraints:

- V_T = 0.3 V (20% of V_{DD}) at L_{EFF} = 1.0 μm.
- $\Delta V_T \leq 200$ mV due L_{EFF}.
- $\Delta V_T \leq 200$ mV due substrate voltage, V_{SUB}.
- $C_J \leq 2$ fF/μm at V_{SUB} = 0 V.
- $I_{SUB} \leq 100$ nA/μm at L_{EFF} = 0.1 μm.
- $gm_{SAT} \geq 100$ mS/mm at L_{EFF} = 0.1 μm.

The second task of the design process is to design a long channel NMOS transistor whose V_T = 0.3 V (20% of the supply voltage). For this task, a former device template file in ATLAS is modified to form a 1.0 μm channel length NMOS transistor structure with a 5nm thick gate oxide, 150 nm thick gate polysilicon and 10^{20} cm^{-3} S/D peak doping concentration. The peak doping concentration as well as the standard deviation of the channel implant is changed until a threshold value of 0.3 V is obtained from the I_D-V_{GS} characteristics at V_{DS} = 50 mV.

Once the channel doping is determined, the third task is to optimize the geometry and the doping concentration of the LDD region. LDD is a region formed to prevent premature impact ionization and resultant hot electrons due to high lateral electric fields at the drain of a short channel transistor [11]. To obtain the optimum LDD region, the shortest transistor (L_{EFF} = 0.1 μm) is formed and the LDD matrix such as in Table I is employed.

Each combination in Table I use the same junction depth and channel doping profile obtained in the first and second tasks, respectively. Each time a different LDD parameter is used; the maximum gm_{SAT} and substrate current, I_{SUB}, are measured and plotted for a 0.1 μm device as shown in Figure 2. All optimum LDD configurations are on the solid line in Figure 2. Since the performance constraints require that a transistor with I_{SUB} less than 100 nA/μm and gm_{SAT} greater than 100 mS/mm should be designed, a LDD configuration with 90 nm length, 50 nm depth and 8x10^{17} cm^{-3} doping concentration is selected as shown by a circle in Figure 2.

The fourth task in this experiment is to determine the change in V_T with respect to L_{EFF} to quantify the charge-sharing ratio, γ . For this purpose, device structures between 0.1 and 1.0 μm channel lengths are constructed. In each structure, the channel, junction and LDD configurations are kept unchanged. Subsequently, V_T from each device is measured and plotted

against L_{EFF} as shown in Figure 3. Here, students are able to observe the effect of charge-sharing ratio, γ , on V_T as mentioned earlier in Experiment 1.

The fifth task is to determine the body effect of this transistor. Body effect is the increase in transistor's threshold voltage with increasing substrate bias, V_{SUB} [12]. This parameter has an important significance on digital circuit performance since a small increase in V_T substantially decreases transistor's current drive capability or gm_{SAT} as seen in (2). This task, however, is essentially an analysis rather than a design since the simulation extracts V_T from an already designed device and plots at elevated substrate biases. Note that the true change in V_T as a function of substrate bias is measured more accurately in a long channel device due to the negligible effect imposed by the charge-sharing factor, γ . The body effect for this particular design was found approximately 170 mV/V, and it is plotted in Figure 4.

Experiment 2 concludes with a final task that measures S/D junction capacitance. C_J is another important factor limiting the performance of a digital circuit composed of a string of transistors connected in series (such as a string of NMOS transistors in a NAND gate or PMOS transistors in a NOR gate). This circuit configuration induces large Elmore gate delays [13] and "slow" output nodes primarily due to C_J. In this task, the small signal capacitance between the source and substrate terminals of a long channel device is measured as a function of substrate voltage. Figure 5 shows the change in C_J of a conventional NMOS transistor as a function of increasing V_{SUB}. This task is also an analysis rather than a design since it extracts C_J from an already designed device.

Experiment 3: Enhancing the transistor performance

So far students are simply expected to follow a methodology that designs a conventional transistor and meets a set of design specifications. From this point forward, students will be asked to make performance enhancements on the existing design using the same technology in experiment 2. The methodology in this experiment is slightly different from the one used in experiment 2: it targets to improve the shortest channel device characteristics first before dealing with longer channel length transistors.

The first device enhancement targets to minimize the charge sharing-effect in short channel devices and keep the V_T drop-off relatively unaffected from decreasing channel lengths. The purpose of this enhancement is to have the maximum current drive capability of the transistor only as a function of W/L_{EFF} but not also a function of V_T for all channel lengths.

The second enhancement aims to reduce or eliminate the bulk effect or the change in V_T with respect to V_{SUB} so that any potential drop between source and bulk contacts should not decrease gm_{SAT}. A transistor connected in series with a chain of transistors is a good candidate suffering from bulk effect.

The final enhancement is to reduce C_J compared to the earlier design. This is another important device issue in digital circuits composed of a chain of transistors towards minimizing the Elmore gate delay and "slow" output nodes.

A new set of performance constraints is given to students as shown below. Note that the value of C_J is specified to be an order of magnitude less compared to the value for conventional NMOS transistors. The technology specifications, on the other hand, are the same as defined in experiment 1.

- $V_T = 0.3$ V (20% of V_{DD}) at $L_{EFF} = 1.0$ µm.
- $\Delta V_T \leq 50$ mV due L_{EFF}.
- $\Delta V_T \leq 50$ mV due substrate voltage, V_{SUB}.
- $C_J \leq 0.2$ fF/µm at $V_{SUB} = 0$ V.
- $I_{SUB} \leq 100$ nA/µm at $L_{EFF} = 0.1$ µm.
- $gm_{SAT} \geq 150$ mS/mm at $L_{EFF} = 0.1$ µm.

At this point, students are expected to go to the library, read related device papers and discuss their findings with the instructor to determine how to design the new transistor. To guide students through this difficult process, we have done a pilot study, which suggests the following ideas for improving the device performance prior to this experiment.

The first idea addresses minimizing V_T roll-off due to the charge sharing affect in short channel transistors. Earlier studies propose a p^+ "halo" formation wrapping around drain and source contacts as one of the solutions to improve charge-sharing effect [14]. However, this structure also increases C_J and promotes hot electron degradation for the gate oxide. Removing p^+ region from under S/D junctions and forming isolated p^+ pockets in adjacent with neighboring n-type LDD regions reduces the charge sharing effect without increasing C_J [15].

The second idea focuses on reducing C_J. A recent study on localizing the channel implant only under the gate can be a viable solution as long as the OFF current requirement for the transistor is not too low. The Local Channel Implantation (LCI) is a fabrication technique to align the threshold implant with the metallurgical gate and prohibit any planar channel

implant from being under the S/D junctions [16].

Reducing the bulk effect is the third idea, which requires the following example: consider the bulk effect of a NMOS transistor with a constant channel doping against a step function channel doping. The step function exhibits high doping concentration at the semiconductor surface and much lower in the bulk. Both transistors have the same V_T when the substrate voltage was equal to 0 V. If V_T of each transistor is calculated as V_{SUB} is changed from 0 to 1.5 V, one observes that the bulk effect of the transistor with a step function channel implant is smaller. In fact, the bulk effect reduces even further with increasing surface doping concentration and decreasing surface doping depth. However, process simulations with high dose, low energy "shallow" Boron implant used as the threshold implant for the channel show that Boron has an implant "tail", which causes a significant bulk effect of its own. Compensating the Boron tail by low-dose, high-energy "deep" Arsenic implant is a possible solution towards eliminating bulk effect [17].

In the pilot study, we combined all these structural design concepts prior to redesigning an improved NMOS transistor. The cross section of this new design for L_{EFF} = 0.2 μm is shown in Figure 6 as an example. The geometry and the doping concentration of the p^+ pocket as well as the LCI region were initially adjusted to have a 0.3 V threshold voltage for a 1.0 μm transistor. During this task, we kept the p^+ pocket length to a minimum just to confine the lateral depletion region within the p^+ pocket but not extending into the channel at V_{DS} = 1.5 V.

Once the p^+ pocket and LCI channel configurations were defined, we applied the LDD matrix in Table I to the 0.1 μm transistor and measured and plotted gm_{SAT} and I_{SUB} for each LDD configuration. The results of this study are shown in Figure 2. The best LDD configurations are on the dashed line in this figure. Since the new specifications require that a transistor with I_{SUB} less than 100 nA/μm and gm_{SAT} greater than 150 mS/mm should be designed, an LDD configuration with 70 nm length, 50 nm depth and $6x10^{17}$ cm^{-3} doping concentration was selected as shown by a circle.

Next, the effect of p^+ pockets on V_T roll-off is determined. Figure 3 shows that ΔV_T value is approximately equal to 45 mV for the new design compared to 125 mV for the conventional transistor.

The reduction in bulk effect is shown in Figure 4. The change in V_T as function of V_{SUB} is found to be 3 mV/V for the enhanced transistor compared to 170 mV/V for the conventional design when the tail of the Boron implant was compensated with Arsenic implant.

The effect of LCI on S/D junction capacitance is shown in Figure 5. The junction capacitance barely changed above 0.2 fF/μm for substrate voltages between 0 and 1.5 V.

However, all these device enhancements came with a price as predicted earlier. The OFF current, I_{OFF}, of the enhanced 0.1 μm NMOS transistor increased more than two orders of magnitude compared to its conventional counterpart. This result is shown in Figure 7. We showed in this pilot study that this was a punch-through effect between the source and drain of the new transistor [9]; I_{OFF} decreased gradually as the substrate concentration or the depth of the LCI region increased. Needless to say that increasing substrate concentration raised S/D junction capacitance and increasing LCI depth increased bulk effect.

In this pilot study, we will not show the method of redesigning the transistor structure to meet the I_{OFF} specifications due to the space requirements of this manuscript. However, we urge course developers to include I_{OFF} as part of the specification list for laboratory experiments.

STUDENT EVALUATION OF THE COURSE AND FEEDBACK

Since this is a pilot study, we have not yet received any student feedback. However, we are glad to say that one of our graduate students started a M.S. thesis on designing a 30 nm effective channel NMOS transistor using the same design methodologies and simulation environment outlined above.

CONCLUSIONS

This graduate laboratory allows students to observe the actual transistor behavior by changing the device parameters. With Silvaco's device design platform, we predict that students will be able to make accurate design trade-offs and optimize the transistor characteristics during laboratory sessions. We believe that students are able to learn the fundamentals of the MOS theory better if the theoretical concepts are accompanied by a device design laboratory. Each laboratory gradually builds up a part of the final design and targets what students should focus on during each experiment. Students also learn different device design methodologies, use their innovative sides to enhance device performance, meet design specifications, and learn to refer to appropriate library resources if needed.

The V_T roll-off, body effect and S/D junction capacitance were considered as the three main transistor parameters in this manuscript to enhance the conventional device performance.

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TABLES AND FIGURES

TABLE I
LDD PARAMETERS FOR L_{EFF} = 0.1 UM TRANSISTOR

LDD doping (cm^{-3})	LDDdepth (nm)	LDD length (nm)
$4x10^{17}$	50	50, 70, 90
$6x10^{17}$	50	50, 70, 90
$8x10^{17}$	50	50, 70, 90
$1x10^{18}$	50	50, 70, 90

FIGURE 1

THE TWO-DIMENSIONAL CROSS SECTION OF A CONVENTIONAL NMOS TRANSISTOR WITH AN EFFECTIVE CHANNEL LENGTH OF 0.2 UM IN ATLAS DEVICE DESIGN SIMULATION ENVIRONMENT

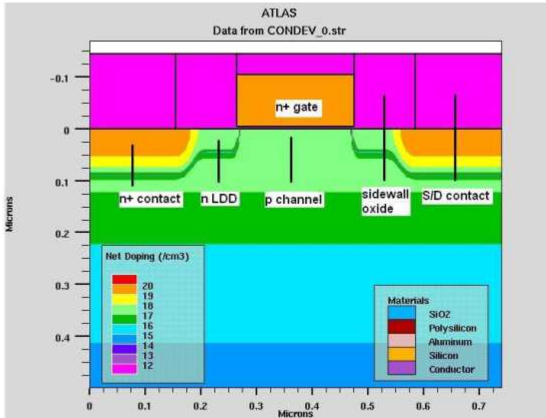

FIGURE 2

MAXIMUM GM_{SAT} VS I_{SUB} FOR THE 0.1 UM CONVENTIONAL AND ENHANCED NMOS TRANSISTOR. CLOSED FIGURES ARE FROM CONVENTIONAL TRANSISTORS AND OPEN FIGURES FROM ENHANCED TRANSISTORS

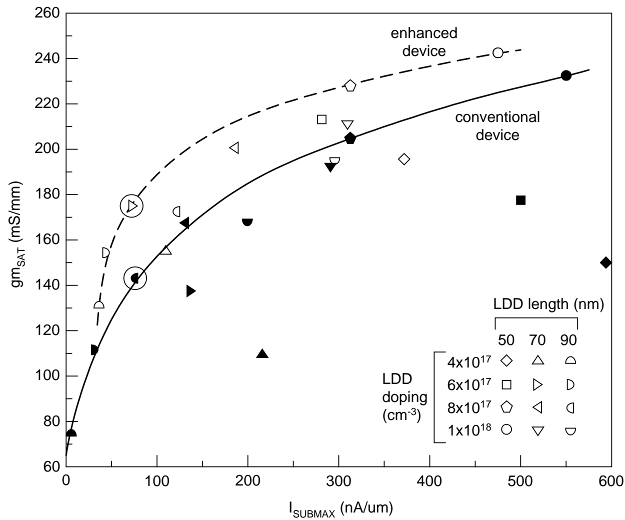

FIGURE 3
THE V_T-ROLL OFF FOR THE CONVENTIONAL AND ENHANCED NMOS TRANSISTORS

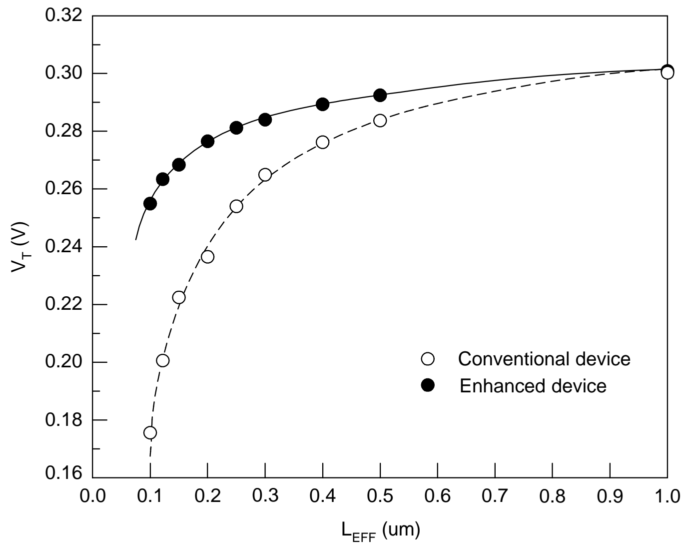

FIGURE 4
BODY EFFECT OF CONVENTIONAL AND ENHANCED NMOS TRANSISTORS FOR $L_{EFF} = 1.0$ UM

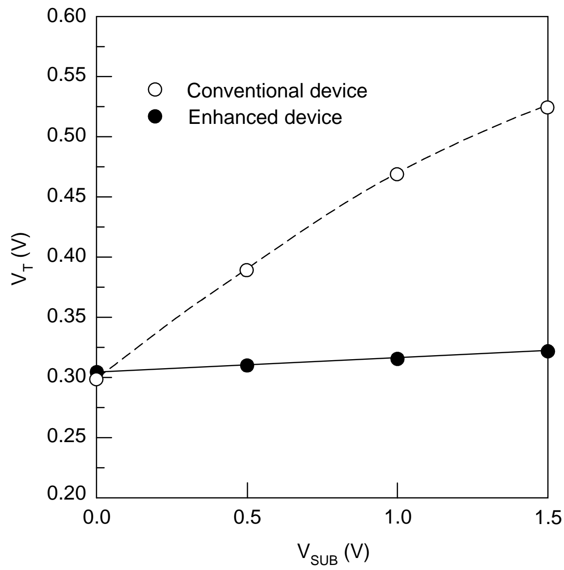

FIGURE 5
S/D JUNCTION CAPACITANCE FOR THE CONVENTIONAL AND ENHANCED NMOS TRANSISTORS AS A FUNCTION OF V_{SUB} AT V_{DS} = 50 MV AND 1.5 V

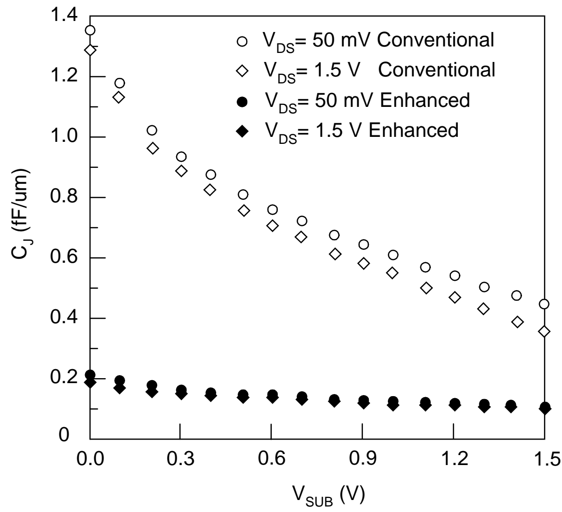

FIGURE 6
THE TWO-DIMENSIONAL CROSS SECTION OF AN ENHANCED NMOS TRANSISTOR WITH AN EFFECTIVE CHANNEL LENGTH OF 0.2 UM IN ATLAS DEVICE DESIGN SIMULATION ENVIRONMENT

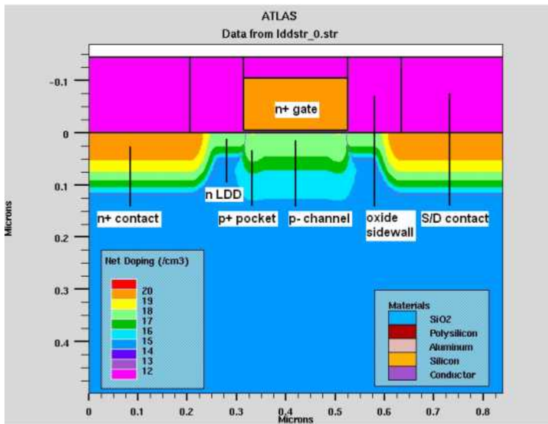

FIGURE 7
I_{OFF} AS A FUNCTION OF L_{EFF}