University and Industry Education/Research Collaboration on Electrostatic Discharge in Microelectronics Devices

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Abstract: This paper presents a long-term education/research collaborative program established between University of Central Florida (UCF) and Intersil Corporation. The collaboration focuses on the topic of electrostatic discharge (ESD) in microelectronics devices and integrated circuits. ESD accounts for more than 25% of microchip failure in semiconductor industry every year. Considering the multi-billion sales generated in the industry every year, the lost revenue associated with the ESD is very high. The capabilities to characterize the ESD event and to design ESD preventive circuits have been a top priority in many semiconductor manufacturing companies. Since the university has the manpower and expertise in fundamental understanding, and industry has the funding resource and training facilities, a program linking the two would be highly desirable. This is the motive behind the collaboration between UCF and Intersil. The background and approaches of the project, as well as the accomplishments resulted from the collaboration, will be described in details.

1. Introduction

Collaboration between university and industry can often result in a research and/or education program that are highly fruitful and mutual beneficial. Since the university has the manpower and expertise in fundamental understanding, and industry has the funding resource and training facilities, a program linking the two would be highly desirable. Through such an interaction, the faculty and student at university receive financial support, have the access to the state-of-art equipment, and are in touch with the practical project in industry. On the other hand, the company gains knowledge and know-how from the research conducted at university, which leads an improvement in the company's products and profits. The collaboration also serves as a training ground for the students, who are often hired by the industry partner after graduation because the students have obtained the proper education background required by the company.

This paper presents an education/research collaborative project between the University of Central Florida, Orlando, Florida, and Intersil Corporation, Melbourne, Florida. The focus of the project is the study of an important failure mechanism in microchips called the electrostatic discharge (ESD). ESD is an event in which a finite amount of charge is transferred between two objects at different potentials. Fig. 1 shows such an event where the electrostatic charge on the metal door knob is transferring to the ground via a human body. For microchips, the main concern of

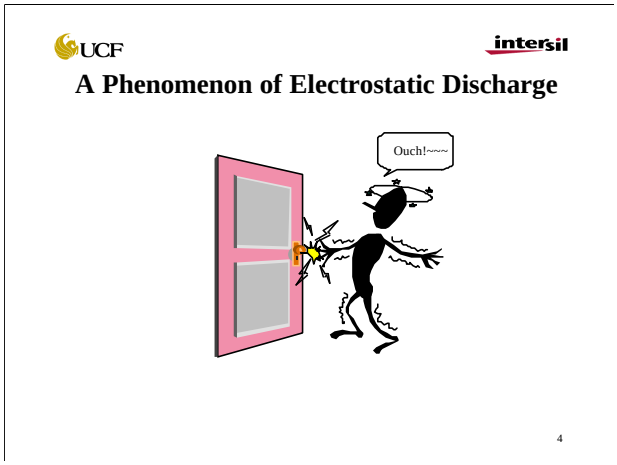

Fig. 1 An ESD event where the charge is transferring to the ground via a human body.

the ESD is opposite and is called the human body model (HBM). Human being has a capacitance of about 100 pF and thus can accumulate electrostatic charge generated from the environment [1]. When touching a microchip, the charge on the human body is transferred to the chip. This resembles a voltage of about 2000 V applied to a resistor of a few hundred ohms, thus resulting a huge current passing through the chip in a very short period of time and consequently damaging the chip [2].

2. Background and Approach

Intersil Corporation, previously known as Harris Semiconductor, is located in Melbourne, Florida. It is one of the leading companies in the United States in manufacturing high-speed and wireless communication systems, which require the use of many state-of-art microchips. Since the percentage of the chip failure due to HBM is quite high, a group of engineers at Intersil has been working on the ESD prevention for many years. The University of Central Florida is located in Orlando, Florida, about 80 miles north of Melbourne. It is one of the ten state universities in Florida, has about 31,000 students in five different colleges. The Electrical and Computer Engineering Dept. is within the College of Engineering and has about 35 faculty and 1000 undergraduate and 250 graduate students. The group of microelectronics in the ECE Dept. has several research laboratories and is actively engaging research on many different subjects.

Realizing the benefits of university and industry collaboration, in early 1995, the microelectronics group at UCF, led by professor J. J. Liou, and the ESD design group at Intersil, headed by Gregg Croft, started the joint project to train students at UCF and to conduct research on the ESD project. At UCF, one faculty, Dr. Liou, and three students, one undergraduate, one M.S., and one Ph.D. student, were involved in the project. At Intersil, a group of three engineers serve as the project mentors and interact with the UCF team on the project.

2.1 Collaboration approach

The approach of the collaboration is described below. Two areas of research are required; one is the development of an improved technique to measure the transient response of the chip subjected to the HBM ESD event, and the other is the numerical simulation of the semiconductor device behavior under the ESD stress. Because it takes time to setup the necessary measurement equipment at UCF, it was mutually agreed to have the Ph.D. student, who has finished all the regular courses at UCF, to move to Melbourne and work at Intersil fulltime. The other two students stay at UCF and conduct device and circuit simulation in the Solid-State Electronics Lab at UCF. The Lab is equipped with several PC's, workstations, and software tools and is sufficient to carry out the project. A project meeting is held once a month to discuss the progress of the project and to determine the future directions.

2.2 Strengths and weaknesses of approach

The strengths of our collaboration approach are:

1) Easy access to the state-of-art equipment at Intersil.
2) Daily interaction between the Ph.D. student and the engineers at Intersil.
3) More evenly distributed mentoring of students; the Ph.D. student is largely supervised by the engineers at Intersil, whereas the undergraduate and M.S. students are supervised by the faculty at UCF.
4) Students are exposed to the practical and important problems related to microelectronics and thus gain good training and experiences before graduating.
5) In addition to the financial support from the collaborative project, the Ph.D. student also receives support from Intersil for attending conferences and training courses.

The weaknesses of our collaboration approaches are:

1) Difficult to communicate with the Ph.D. student working off campus.
2) The engineers at Intersil have less experiences on supervising fundamental research.
3) Conflicting research directions suggested by the faculty at UCF and engineers at Intersil.
4) Difficult to consolidate the simulation work at UCF and characterization work at Intersil.
5) Different priorities and emphases seen by university and industry. The team at UCF places more emphasis on the fundamental understanding of the ESD in microchip and on publications, whereas the team at Intersil is more interested in solving problems related to the manufacturing and operation.

3. Accomplishments To -Date

3.1 Research accomplishment

A great deal of research work has been accomplished through the collaborative efforts. Below are two examples of research accomplishment.

3.1.1 Improved experimental setup for ESD measurements

In testing and characterizing the microchip performance, it is imperative to have an accurate and effective experimental setup. This is particularly true for the transient measurements of ESD event due to its very high current within a very short period of time (a few hundred pico seconds). A technique called the transmission line pulsing (TLP) technique is often used in the ESD measurements, and a schematic of the ESD measurement setup using the TLP is shown in Fig. 2. Ideally, the TLP technique generates a square-shape pulse, which resembles the HBM ESD and is applied to the microchip under test. A main problem is that the pulses generated from the TLP are often distorted and oscillatory, as can be seen in Fig. 3.

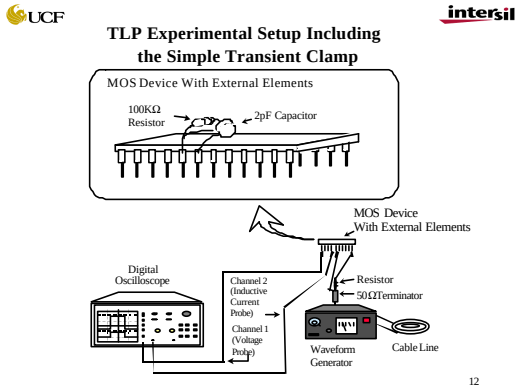

Fig. 2 ESD measurement setup using TLP technique

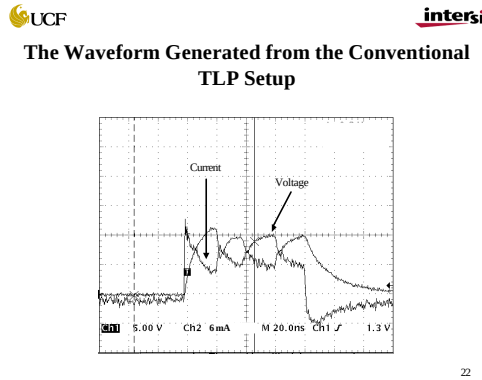

Fig. 3 Distroted pulses generated from the typical TLP setup.

In the course of our collaborative research, we have developed an improved experimental TLP setup that generates well-shaped TLP pulses [3]. The setup is illustrated in Fig. 4, which consists of an improved voltage probe and an improved matching load circuit. The pulses generated from this setup are much improved, as shown in Fig. 5.

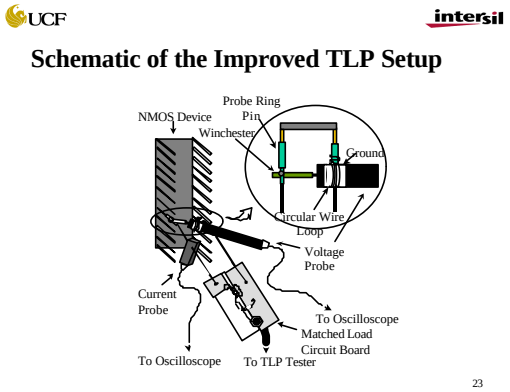

Fig. 4 Improved TLP setup

Three Stages

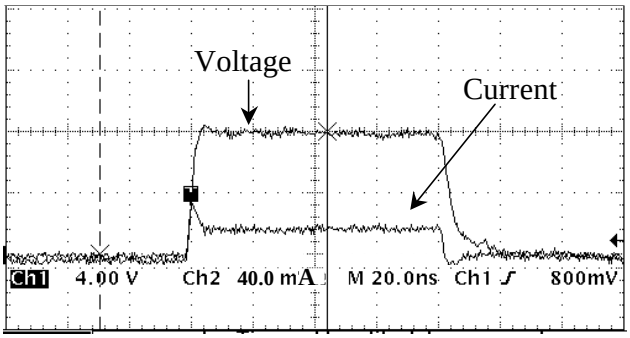

Fig. 5 Pulses generated from the improved TLP setup.

3.1.2 Improved MOS model for ESD circuit simulation

A transistor called the metal-oxide-semiconductor field-effect transistor (MOSFET) is frequently used in microchips, and a ESD model for the MOSFET is needed to simulate the behavior of the microchips under the ESD event. Fig. 6 shows that behavior of a typical MOSFET drain current versus drain voltage characteristics under the ESD obtained from measurements and from the conventional MOSFET model. The characteristics where the drain current increases almost vertically, a phenomenon called the snapback, is the region of ESD operation. Clearly, the error of the conventional model is significant when the MOSFET is subjected to the ESD stress. The reason for this inaccuracy stems from the fact that the conventional MOSFET model neglected the parasitic bipolar transistor existed in the MOSFET [4]. Under the normal operation (i.e., small drain voltages), the parasitic bipolar transistor is inactive. During the ESD event, however, the drain voltage is high and such a transistor is turned on because of the voltage drop in the substrate region of the MOSFET caused by a large leakage current passing through the region. The directions of the electron and hole flows in the MOSFET during ESD are illustrated in Fig. 7. This results in a rapid increase in the drain current at the high drain voltage region (i.e., snapback region). Based on this device physics and the understanding of the ESD, we have developed an improved MOSFET model, and the comparison of model predictions against measurements is given in Fig. 8.

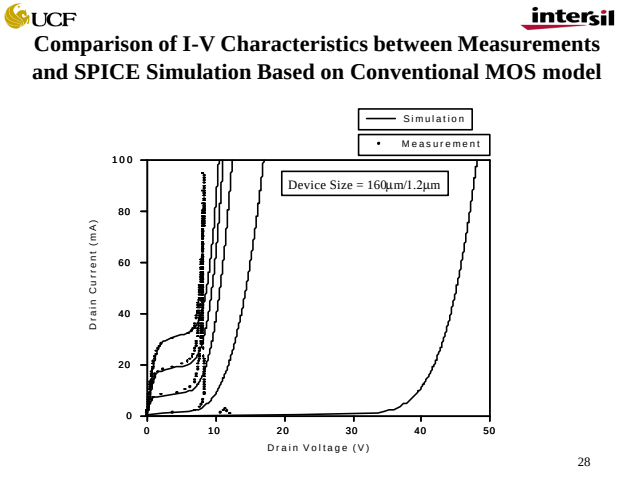

Fig. 6 Current-voltage characteristics of MOSFET under the ESD obtained from measurements and conventional MOSFET model.

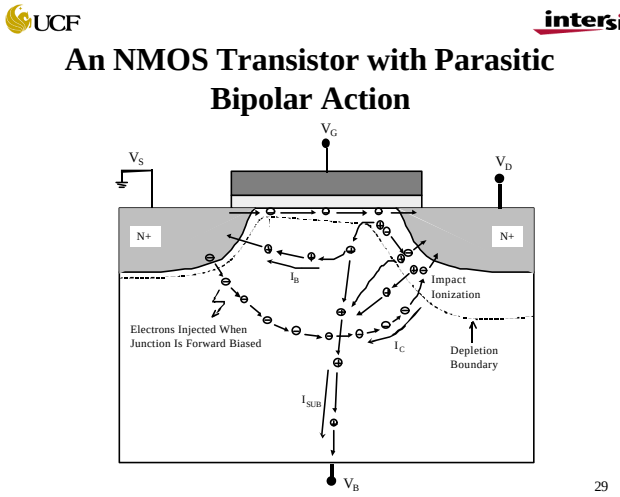

Fig. 7 Flows of electrons and holes in MOSFET during the ESD event.

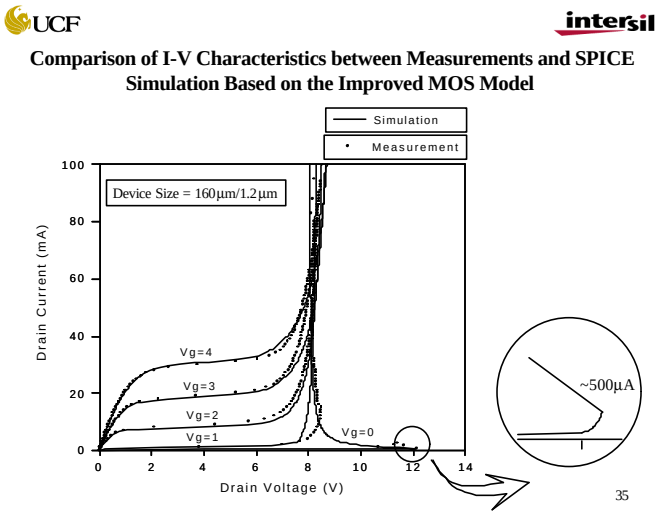

Fig. 8 Current-voltage characteristics of MOSFET under the ESD obtained from measurements and improved MOSFET model.

3.2 Education accomplishment

The accomplishments on education can be summarized below.

1) One Ph.D., one M.S., and one undergraduate students have graduated under the sponsorship of the collaboration project.
2) Excellent training to the students on the subjects of ESD in microchips.
3) A lab has been setup at UCF to carry out the testing and characterization of ESD in microchips.
4) A new graduate-level course has been developed and established at UCF. The course covers the subject of wireless communications and is taught at UCF by engineers from Intersil.

4. Conclusions

A university and industry research/education collaborative program established between the University of Central Florida and Intersil Corporation was presented. The subject of the study is electrostatic discharge in semiconductor devices and integrated circuits. The background and infrastructure of our collaboration were discussed, and the strengths and

weaknesses of the approach addressed. In addition, the research and education work accomplished to-date was presented. The paper provides a useful example on how university and industry can be collaborated fruitfully and mutual beneficially.

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5. References

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